1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,MLB,X970

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
2			2019-06-19

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19	19	Chipset Support 1	ARMIN	01/17/2019
20	20	Chipset Support 2	ANDY	02/19/2019
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40	41	SoC ISP/I2C/UART/SPI/I2S		01/17/2019
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46	47	SoC Shared Support	ARMIN	01/17/2019
47	48	SoC Project Support	ANDY	02/19/2019
48	49	MESA	ARMIN	01/17/2019
49	50	SECURE ELEMENT	ANDY	02/19/2019
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60	62	Audio Placeholder		01/17/2019
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75	78	PMIC BUCKS AND SWs		01/17/2019
76	79	PMIC LDOs	ARMIN	01/17/2019
77	80	PMIC GPIOs & Control		01/17/2019
78	81	VR VCCIO		01/17/2019
79	82	Power FETs	ARMIN	01/17/2019
80	83	SOC/PMIC Aliases	ARMIN	01/17/2019
81	84	LCD Backlight Driver		01/17/2019
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91	94	SSD0 S4E 3		01/17/2019
92	95	SSD0 PMIC & VR		01/17/2019
93	96	GPU VRAM CHs A, B	J187_ALAN	09/18/2018
94	97	GPU VRAM CHs C, D	J187_ALAN	09/18/2018
95	98	EDP Mux		08/22/2018
96	99	GPU PCC / Sensors	J780	08/22/2018
97	100	GPU Navi14 PCIe / DP A / Misc	SEAN	08/22/2018
98	101	GPU Navi14 DP / GPIO / Debug		08/22/2018
99	102	GPU Navi14 Power	SEAN	08/22/2018
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106	109	GPU 1.8V / 0.75V	SEAN	08/22/2018
107	110	USB-C HIGH SPEED 1	YANIR	01/17/2019
108	111	USB-C HIGH SPEED 2	ANDY	01/17/2019
109	112	USB-C T Support	YANIR	01/17/2019
110	113	USB-C PORT CONTROLLER TA	YANIR	01/17/2019
111	114	USB-C PORT CONTROLLER TB	YANIR	01/17/2019
112	115	USB-C T CONNECTOR	YANIR	01/17/2019
113	116	USBC T Connector Support	ANDY	03/26/2019
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117	120	Power Alias 1	ZIFENG	01/17/2019
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119	122	Signal Alias		01/17/2019
120	123	High speed No Testpoints	ANDY	01/17/2019
121	124	DFU TEST POINTS	ANDY	01/17/2019
122	125	FCT TESTPOINTS 2	ANDY	01/17/2019
123	126	ICT, MAC-1, & EE Testpoints	ANDY	03/26/2019
124	127	Desense Caps 1	ZIFENG	08/22/2018
125	128	Desense Caps 2	ZIFENG	10/14/2018
126	129	Desense Caps 3	ZIFENG	08/22/2018
127	130	Desense Caps 4	ZIFENG	06/05/2019
128	131	Memory Bite/Byte Swizzle		01/17/2019
129	140	Debug	ANDY	10/14/2018
130	141	BOM 639 XTA		10/14/2018
131	143	BOM 639 XLA		10/14/2018
132	144	BOM 639 MISC		10/14/2018
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ABBREV=ABBREV
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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-04492	1	SCHEM,MLB-NAVI,X970	SCH	CRITICAL	SCH
820-01700	1	PCBF,MLB-NAVI,X970	PCB	CRITICAL	PCB

SYNC_MASTER=ZIFENG SYNC_DATE=08/22/2018

DRAWING TITLE
SCHEM,MLB-NAVI,X970

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X970 BOM Groups

BOM GROUP	BOM OPTIONS
SSD_LANDS:6	ALTERNATE,S4E_L6
SSD_LANDS:7	ALTERNATE,S4E_L6,S4E_L7
SSD_LANDS:8	ALTERNATE,S4E_L6,S4E_L7,S4E_L8
X970_COMMON	SCH,PCB,COMMON,ALTERNATE,COMMON1,COMMON2,COMMON3,PROGPARTS
COMMON1	CPUPEG:X8X4X4,EDP:YES,BOARD_ID:0X3A,SE:DEV_2019,EN_VP0R_LPS:YES
COMMON2	PCC:YES,RF_TUNING,BOARD_REV:010,BAT_I2C:3V3
COMMON3	SKIP_5V3V3:AUDIBLE,XDP:YES,VCCSPI:3V3,SVID_PU:CORE
SNS	LOADISNS,LOADRC:YES,SENSOR:DEV
DEVEL:ENG	ALTERNATE,SNS,DBGLED,XDP_CONN,USBC_DBG,DBG_BTN,WIFI_DBG,BOOTCFG0,ESPI_DBG
DEVEL:PVT	ALTERNATE,LOADRC:NO

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00271	COMMON PARTS,MLB-NAVI,X970	X970_COMMON
685-00308	ITLC 6L Parts,MLB-NAVI,X970	SSD_LANDS:6
685-00309	ITLC 7L Parts,MLB-NAVI,X970	SSD_LANDS:7
685-00310	ITLC 8L Parts,MLB-NAVI,X970	SSD_LANDS:8
985-00889	DEV PARTS,MLB-NAVI,X970	DEVEL:ENG
685-00296	VRAM PARTS,MICRON,4GB,MLB-NAVI,X970	VRAM:MC-4GB
685-00297	VRAM PARTS,SAMSUNG,4GB,MLB-NAVI,X970	VRAM:SS-4GB
685-00298	VRAM PARTS,HYNIX,8GB,MLB-NAVI,X970	VRAM:HY-8GB
685-00299	VRAM PARTS,MICRON,8GB,MLB-NAVI,X970	VRAM:MC-8GB
685-00300	VRAM PARTS,SAMSUNG,8GB,MLB-NAVI,X970	VRAM:SS-8GB

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
685-00271	1	COMMON PARTS,MLB-NAVI,X970	BASE	CRITICAL	BOM_BASE
685-00308	1	ITLC 6L Parts,MLB-NAVI,X970	6L	CRITICAL	SSD_BOM:6L
685-00309	1	ITLC 7L Parts,MLB-NAVI,X970	7L	CRITICAL	SSD_BOM:7L
685-00310	1	ITLC 8L Parts,MLB-NAVI,X970	8L	CRITICAL	SSD_BOM:8L
985-00889	1	DEV PARTS,MLB-NAVI,X970	DEVEL	CRITICAL	BOM_DEV

Memory Options

BOM GROUP	BOM OPTIONS
MEM:HY-16GB	DRAM:HY-16GB,RAMCFG0:L
MEM:MC-16GB	DRAM:MC-16GB,RAMCFG1:L
MEM:HY-32GB	DRAM:HY-32GB,RAMCFG3:L,RAMCFG0:L
MEM:MC-32GB	DRAM:MC-32GB,RAMCFG3:L,RAMCFG1:L
MEM:MC-64GB	DRAM:MC-64GB,RAMCFG2:L,RAMCFG1:L

VRAM Options

BOM GROUP	BOM OPTIONS
VRAM:MC-4GB	VRAM_SIZE:4GB,VRAM_IC:MC-4GB
VRAM:SS-4GB	VRAM_SIZE:4GB,VRAM_IC:SS-4GB
VRAM:HY-8GB	VRAM_SIZE:8GB,VRAM_IC:HY-8GB
VRAM:MC-8GB	VRAM_SIZE:8GB,VRAM_IC:MC-8GB
VRAM:SS-8GB	VRAM_SIZE:8GB,VRAM_IC:SS-8GB

SSD Options

BOM GROUP	BOM OPTIONS
SSD:TS-256	SSD_NAND:TS-256,SOC:1GB,JTAG:L5
SSD:WD-256	SSD_NAND:WD-256,SOC:1GB,JTAG:L5
SSD:TS-512	SSD_NAND:TS-512,SOC:1GB,JTAG:L5
SSD:SS-512	SSD_NAND:SS-512,SOC:1GB,JTAG:L5
SSD:WD-512	SSD_NAND:WD-512,SOC:1GB,JTAG:L5
SSD:TS-1TB	SSD_NAND:TS-1TB,SOC:2GB,JTAG:L6,SSD_BOM:6L
SSD:WD-1TB	SSD_NAND:WD-1TB,SOC:2GB,JTAG:L6,SSD_BOM:6L
SSD:TS-2TB	SSD_NAND:TS-2TB,SOC:2GB,JTAG:L7,SSD_BOM:7L
SSD:WD-2TB	SSD_NAND:WD-2TB,SOC:2GB,JTAG:L7,SSD_BOM:7L
SSD:HY-4TB	SSD_NAND:HY-4TB,SOC:2GB,SSD_BOM:8L
SSD:WD-4TB	SSD_NAND:WD-4TB,SOC:2GB,SSD_BOM:8L
SSD:WD-8TB	SSD_NAND:WD-8TB,SOC:2GB,SSD_BOM:8L

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Board ID[7:0] = 8b'00111010 = 8h'3A

BOM GROUP	BOM OPTIONS
BOARD_ID:0X3A	BOARDID5,BOARDID4,BOARDID3,BOARDID1

SYNC_MASTER= SYNC_DATE=06/22/2018

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CPU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S00722	1	CPU,CFLH,SRF6U,PRQ,2.6,1.15,6C,BGA1440	U0500	CRITICAL	CPU:6C-2.6G
337S00731	1	CPU,CFLH,SRFD1,PRQ,2.3,1.2,8C,BGA1440	U0500	CRITICAL	CPU:8C-2.3G
337S00724	1	CPU,CFLH,SRFD0,PRQ,2.4,1.25,8C,BGA1440	U0500	CRITICAL	CPU:8C-2.4G
998-12472	1	INTERPOSER,CFL-H,BGA1440	U0500	CRITICAL	CPU:INTERPOSER

DRAM

Note: Two rows per part for legibility

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S00200	8	IC,DDR4-2666,8GBIT,19NM,H,BGA78	U2300,U2310,U2320,U2330,U2400,U2410,U2420,U2430	CRITICAL	DRAM:HY-16GB
333S00200	8	IC,DDR4-2666,8GBIT,19NM,H,BGA78	U2500,U2510,U2520,U2530,U2600,U2610,U2620,U2630	CRITICAL	DRAM:HY-16GB
333S00163	8	IC,DDR4-2666,8GBIT,Z11B,18NM,M,BGA78	U2300,U2310,U2320,U2330,U2400,U2410,U2420,U2430	CRITICAL	DRAM:MC-16GB
333S00163	8	IC,DDR4-2666,8GBIT,Z11B,18NM,M,BGA78	U2500,U2510,U2520,U2530,U2600,U2610,U2620,U2630	CRITICAL	DRAM:MC-16GB
333S00201	8	IC,DDR4-2666,16GBIT,19NM,H,BGA78	U2300,U2310,U2320,U2330,U2400,U2410,U2420,U2430	CRITICAL	DRAM:HY-32GB
333S00201	8	IC,DDR4-2666,16GBIT,19NM,H,BGA78	U2500,U2510,U2520,U2530,U2600,U2610,U2620,U2630	CRITICAL	DRAM:HY-32GB
998-18917	8	IC,DDR4-3200,16GBIT,16NM,ES,M,BGA78	U2300,U2310,U2320,U2330,U2400,U2410,U2420,U2430	CRITICAL	DRAM:MC-32GB
998-18917	8	IC,DDR4-3200,16GBIT,16NM,ES,M,BGA78	U2500,U2510,U2520,U2530,U2600,U2610,U2620,U2630	CRITICAL	DRAM:MC-32GB
998-18918	8	IC,DDR4-3200,32GBIT,16NM,ES,M,BGA78	U2300,U2310,U2320,U2330,U2400,U2410,U2420,U2430	CRITICAL	DRAM:MC-64GB
998-18918	8	IC,DDR4-3200,32GBIT,16NM,ES,M,BGA78	U2500,U2510,U2520,U2530,U2600,U2610,U2620,U2630	CRITICAL	DRAM:MC-64GB

GPU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S00719	1	GPU,AMD,NAVI14,ULA,A0,ES,BGA1125	UA000	CRITICAL	GPU:ULA
337S00720	1	GPU,AMD,NAVI14,PROA,A0,ES,BGA1125	UA000	CRITICAL	GPU:PRA
998-19127	1	GPU,AMD,NAVI14,ULA,A0,ES,TDP,BGA1125	UA000	CRITICAL	GPU:TDP
998-19125	1	GPU,AMD,NAVI14,ULA,A0,ES,FF,PSL,BGA1125	UA000	CRITICAL	GPU:UFS
998-19126	1	GPU,AMD,NAVI14,ULA,A0,ES,SS,PSL,BGA1125	UA000	CRITICAL	GPU:USS
998-19109	1	GPU,AMD,NAVI14,ULA,A0,ES,FF,MTAG,BGA1125	UA000	CRITICAL	GPU:UFU
998-19110	1	GPU,AMD,NAVI14,ULA,A0,ES,SS,MTAG,BGA1125	UA000	CRITICAL	GPU:USU
998-19111	1	NAVI14 ADPTR,VDDGFX,VDDSOC,D406	UA000	CRITICAL	GPU:ADPTR_VDDCR
998-19112	1	NAVI14 ADPTR,VDDCI,MVDD,D407	UA000	CRITICAL	GPU:ADPTR_VMEM

VRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S00209	4	IC,GDDR6,8GBIT,14GBPS,1.35V,18NM,M,BG180	U9600,U9610,U9700,U9710	CRITICAL	VRAM_IC:MC-4GB
333S00210	4	IC,GDDR6,8GBIT,14GBPS,1.35V,18NM,S,BG180	U9600,U9610,U9700,U9710	CRITICAL	VRAM_IC:SS-4GB
333S00211	4	IC,GDDR6,16GBIT,14GBPS,1.35V,19NM,H,B180	U9600,U9610,U9700,U9710	CRITICAL	VRAM_IC:HY-8GB
333S00212	4	IC,GDDR6,16GBIT,14GBPS,1.35V,16NM,M,B180	U9600,U9610,U9700,U9710	CRITICAL	VRAM_IC:MC-8GB
333S00213	4	IC,GDDR6,16GBIT,14GBPS,1.35V,18NM,S,B180	U9600,U9610,U9700,U9710	CRITICAL	VRAM_IC:SS-8GB

PCH CNL-H

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S00552	1	IC,CNL PCH-H,USFF,SR40F,PRQ,BGA499	U1200	CRITICAL	

ACE & Ridges

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00441	2	IC,TBT,TITAN RIDGE DP,SLMHS,PRQ,C1,CSP337	U2800,UB000	CRITICAL	
353S01960	4	IC,CD3217,ACE2,B2,USB PWR SW W/HV,BGA123	U3100,U3200,UB300,UB400	CRITICAL	

Power Controllers

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S01525	1	IC,ISL9240HIB0Z,PMU,SOUNA,WCSP40,2.1X3.3MM	U7000	CRITICAL	
353S00928	1	IC,ISL95828A,IMVP8 CPU REG,QFN40,6X6MM	U7100	CRITICAL	
338S00267	1	IC,PMU,CALPE,D2249A0,OTP-AI,CSP324,0.4P	U7800	CRITICAL	
353S02108	1	IC,RAA225101A2,SVI2,CONTROLLER,QFN40,5X5	UA600	CRITICAL	
353S01660	1	IC,SUPPLY,INTERSIL,ISL6277B,SVI2.0,QFN48	UA800	CRITICAL	

WIFI/BT Module & Alternate

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S00609	1	IC,MODULE,WIFI/BT,MURATA,HARPOON,M,ES7.7,LGA385	U3730	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00610	339S00609	ANY	ALL	WIFI/BT Module

Programmable Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S01435	1	TBT-X,R0 (VXXXX) PROTO-3,X970	U2890	CRITICAL	
341S01436	1	TBT-T,R1 (VXXXX) PROTO-3,X970	UB090	CRITICAL	
341S01434	1	ROM,BT SFLASH (V37) PROTO-3,X970	U3750	CRITICAL	
341S00725	1	WIFI ROM (V01) WW1,X665	U3710	CRITICAL	
341S01403	1	ROM,VBIOS,NAVI-14,PROA (VXXX) P-0-A,X970	UA130	CRITICAL	GPU:PRA
341S01404	1	ROM,VBIOS,NAVI-14,ULA (VXXX) P-0-A,X970	UA130	CRITICAL	GPU:ULA

H9M & Alternates

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S00373	1	POP,GIBRALTAR+2GB 21NM,H,B0,SCK,CSP1406	U3900	CRITICAL	SOC:2GB
339S00371	1	POP,GIBRALTAR+1GB 21NM,H,B0,ATK,CSP1406	U3900	CRITICAL	SOC:1GB

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00372	339S00373	ANY	ALL	H9M 2GB
339S00377	339S00373	ANY	ALL	H9M 2GB
339S00378	339S00373	ANY	ALL	H9M 2GB
339S00376	339S00371	ANY	ALL	H9M 1GB
339S00370	339S00371	ANY	ALL	H9M 1GB
339S00375	339S00371	ANY	ALL	H9M 1GB

SSD NAND

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-16395	5	NAND,3DV4,64GBT,S4E,256G,T,SUB Y,SLGA110	U8600,U9100,U9200,U9300,U9400	CRITICAL	SSD_NAND:TS-256
998-16969	5	NAND,3DV4,64GBT,S4E,256G,SD,SUBY,SLGA110	U8600,U9100,U9200,U9300,U9400	CRITICAL	SSD_NAND:WD-256
998-16397	5	NAND,3DV4,128GBT,S4E,256G,T,SUBY,SLGA110	U8600,U9100,U9200,U9300,U9400	CRITICAL	SSD_NAND:TS-512
335S00424	5	NAND,3DV5,128GBT,S4E,256G,SS,SLGA110	U8600,U9100,U9200,U9300,U9400	CRITICAL	SSD_NAND:SS-512
998-16970	5	NAND,3DV4,128GBT,S4E,256G,SD,SBY,SLGA110	U8600,U9100,U9200,U9300,U9400	CRITICAL	SSD_NAND:WD-512
335S00395	6	NAND,3DV4,192GBT,XXX,S4E,256G,T,SLGA110	U8600,U8700,U9100,U9200,U9300,U9400	CRITICAL	SSD_NAND:TS-1TB
335S00407	6	NAND,3DV4,192GBT,XXX,S4E,256G,H,SLGA110	U8600,U8700,U9100,U9200,U9300,U9400	CRITICAL	SSD_NAND:WD-1TB
335S00395	1	NAND,3DV4,192GBT,XXX,S4E,256G,T,SLGA110	U8800	CRITICAL	SSD_NAND:TS-2TB
335S00397	6	NAND,3DV4,320GBT,XXX,S4E,256G,T,SLGA110	U8600,U8700,U9100,U9200,U9300,U9400	CRITICAL	SSD_NAND:TS-2TB
335S00407	1	NAND,3DV4,192GBT,XXX,S4E,256G,H,SLGA110	U8800	CRITICAL	SSD_NAND:WD-2TB
335S00408	6	NAND,3DV4,320GBT,XXX,S4E,256G,SD,SLGA110	U8600,U8700,U9100,U9200,U9300,U9400	CRITICAL	SSD_NAND:WD-2TB
335S00380	8	NAND,3DV4,512GBT,S4E,256G,H,SLGA110	U8600,U8700,U8800,U8900,U9100,U9200,U9300,U9400	CRITICAL	SSD_NAND:HY-4TB
335S00391	8	NAND,3DV4,512GBT,XXX,S4E,256G,SD,SLGA110	U8600,U8700,U8800,U8900,U9100,U9200,U9300,U9400	CRITICAL	SSD_NAND:WD-4TB
335S00433	8	NAND,3DV4,1TBT,XXX,S4E,512G,SD,SLGA110	U8600,U8700,U8800,U8900,U9100,U9200,U9300,U9400	CRITICAL	SSD_NAND:WD-8TB

SSD NAND Substrate Alts

Sub1 Sub2

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
998-16394	998-16395	ANY	ALL	SSD NAND: TB_256
998-16944	998-16969	ANY	ALL	SSD NAND: WD_256
998-16396	998-16397	ANY	ALL	SSD NAND: TB_512
998-16945	998-16970	ANY	ALL	SSD NAND: WD_512

Plasma Cleaned POR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
998-18459	335S00391	ANY	ALL	SSD NAND: WD-4TB Plasma

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PAGE TITLE
BOM Configuration 2

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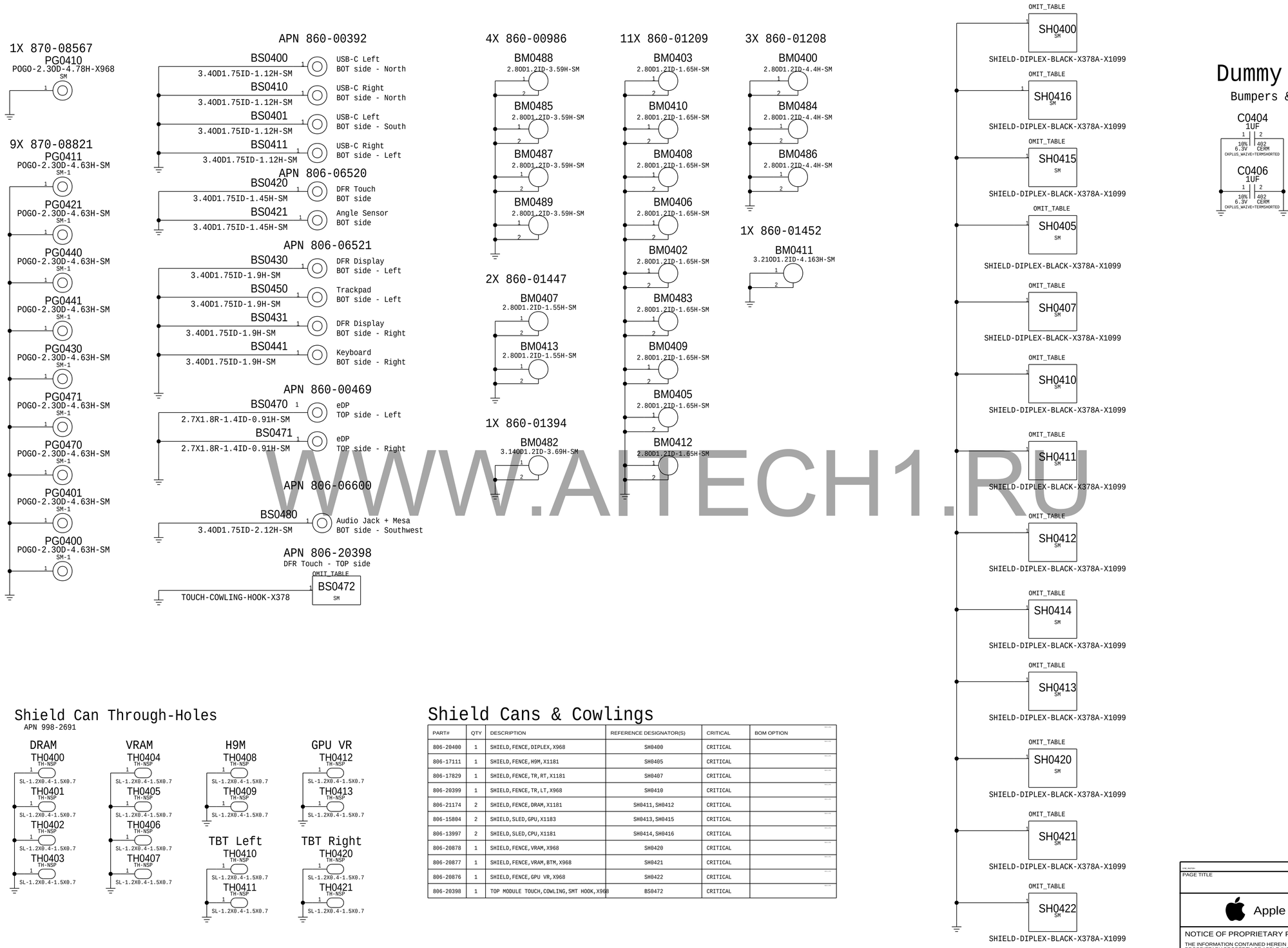

Shield Cans & Cowlings

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-20400	1	SHIELD,FENCE,DIPLEX,X968	SH0400	CRITICAL	
806-17111	1	SHIELD,FENCE,H9M,X1181	SH0405	CRITICAL	
806-17829	1	SHIELD,FENCE,TR,RT,X1181	SH0407	CRITICAL	
806-20399	1	SHIELD,FENCE,TR,LT,X968	SH0410	CRITICAL	
806-21174	2	SHIELD,FENCE,DRAM,X1181	SH0411,SH0412	CRITICAL	
806-15804	2	SHIELD,SLED,GPU,X1183	SH0413,SH0415	CRITICAL	
806-13997	2	SHIELD,SLED,CPU,X1181	SH0414,SH0416	CRITICAL	
806-20878	1	SHIELD,FENCE,VRAM,X968	SH0420	CRITICAL	
806-20877	1	SHIELD,FENCE,VRAM,BTM,X968	SH0421	CRITICAL	
806-20876	1	SHIELD,FENCE,GPU VR,X968	SH0422	CRITICAL	
806-20398	1	TOP MODULE TOUCH,COWLING,SMT HOOK,X968	BS0472	CRITICAL	

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PD Parts

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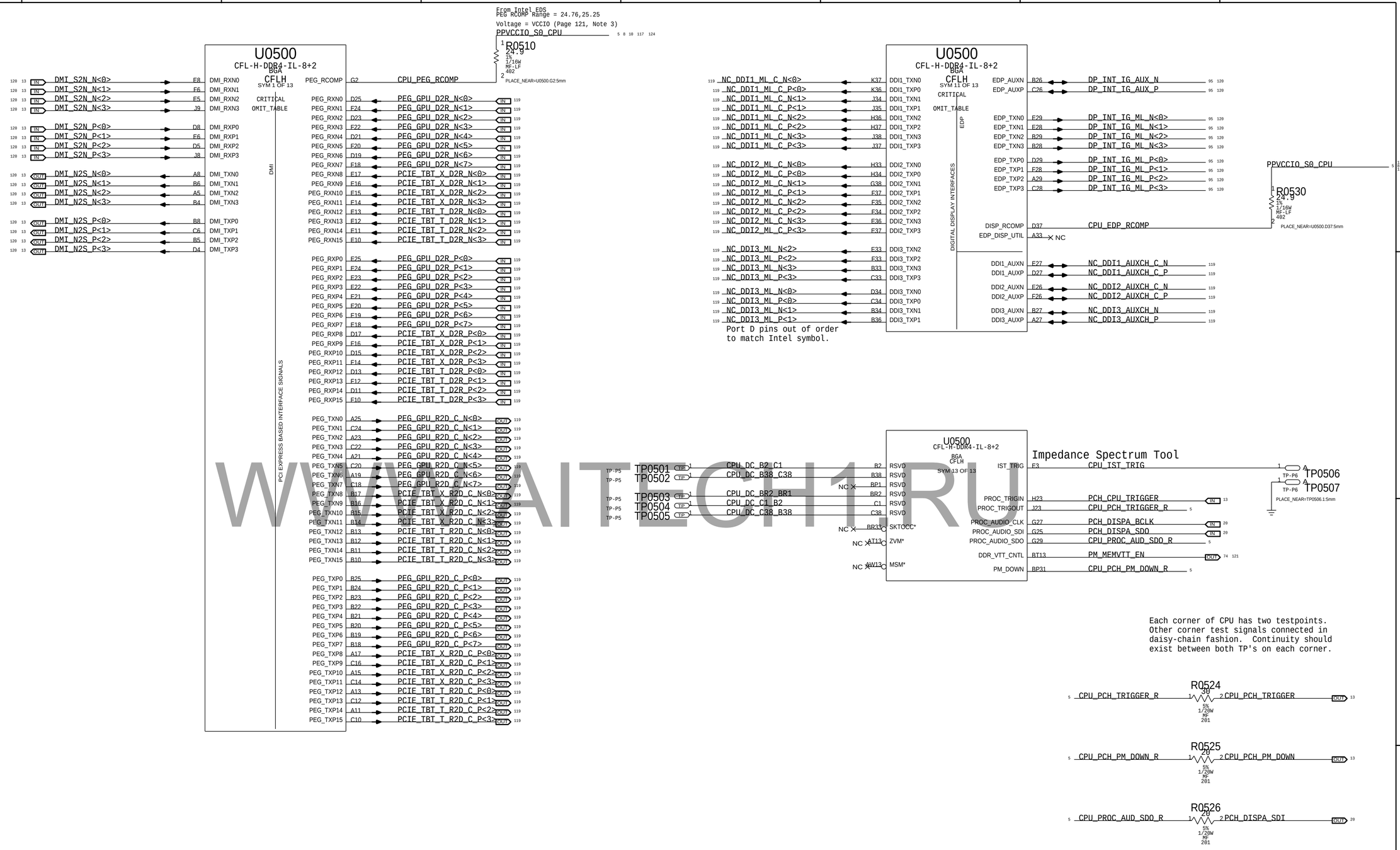

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BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

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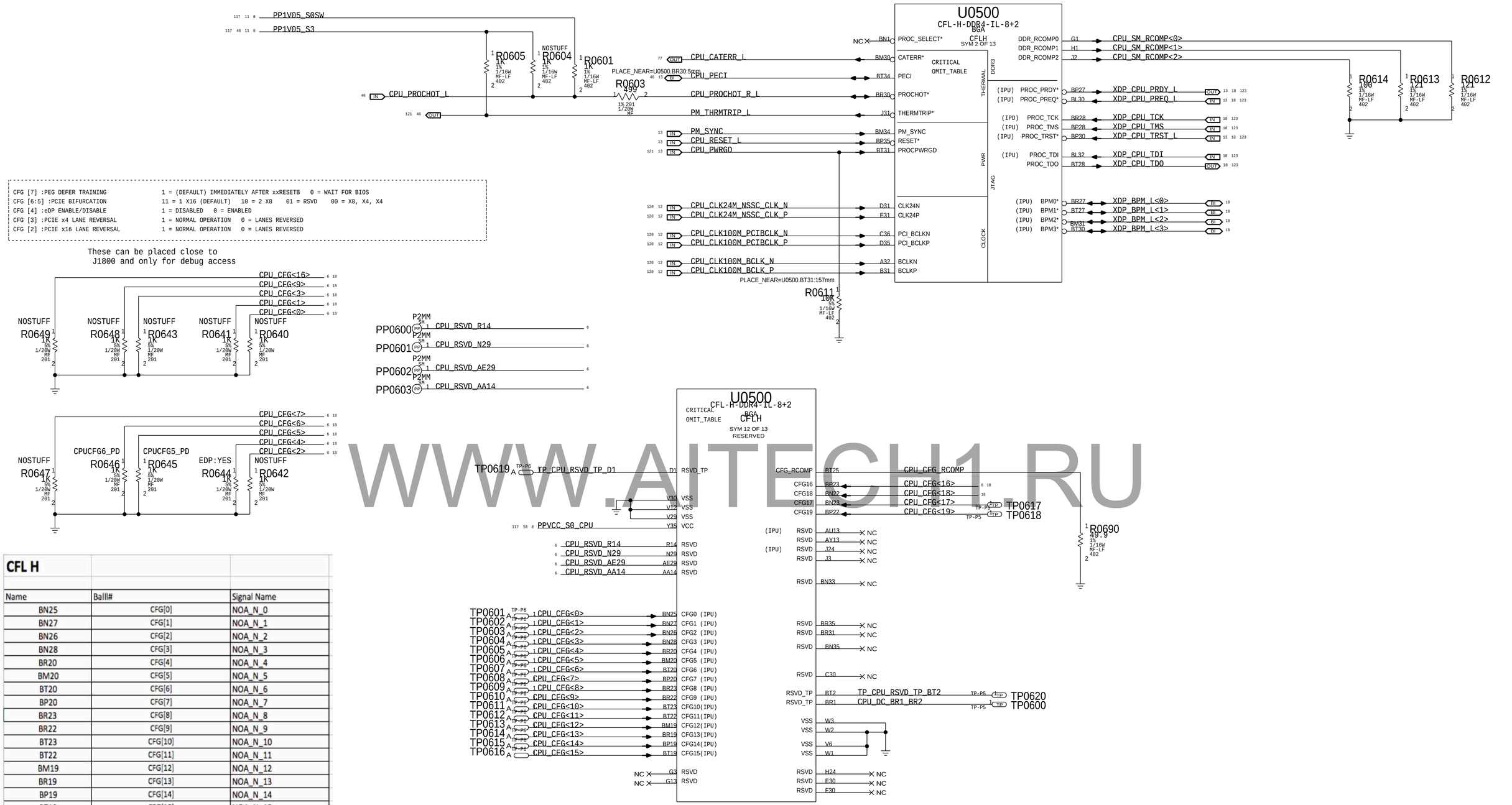

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CFL H

Name	Ball#	Signal Name
BN25	CFG[0]	NOA_N_0
BN27	CFG[1]	NOA_N_1
BN26	CFG[2]	NOA_N_2
BN28	CFG[3]	NOA_N_3
BR20	CFG[4]	NOA_N_4
BM20	CFG[5]	NOA_N_5
BT20	CFG[6]	NOA_N_6
BP20	CFG[7]	NOA_N_7
BR23	CFG[8]	NOA_N_8
BR22	CFG[9]	NOA_N_9
BT23	CFG[10]	NOA_N_10
BT22	CFG[11]	NOA_N_11
BM19	CFG[12]	NOA_N_12
BR19	CFG[13]	NOA_N_13
BP19	CFG[14]	NOA_N_14
BT19	CFG[15]	NOA_N_15
BN23	CFG[17]	NOA_STB_P_0
BP22	CFG[19]	NOA_STB_P_1
D1	RSVD_TP	PEG_VIEW0
E1	RSVD_TP	PEG_VIEW1
E2	RSVD_TP	PEG_VIEW3
E3	IST_TRIG	PEG_VIEW2
BT2	RSVD_TP	DDR_VIEW1
BR1	RSVD_TP	DDR_VIEW0

BOM GROUP	BOM OPTIONS
CPUPEG:X8X8	CPUCFG5_PD
CPUPEG:X8X4X4	CPUCFG6_PD,CPUCFG5_PD

To use PEG X16 configuration, simply remove CPUPEG:X8X8 and CPUPEG:X8X4X4 from BOMs.

PAGE TITLE
CPU Clock/Misc/JTAG/CFG

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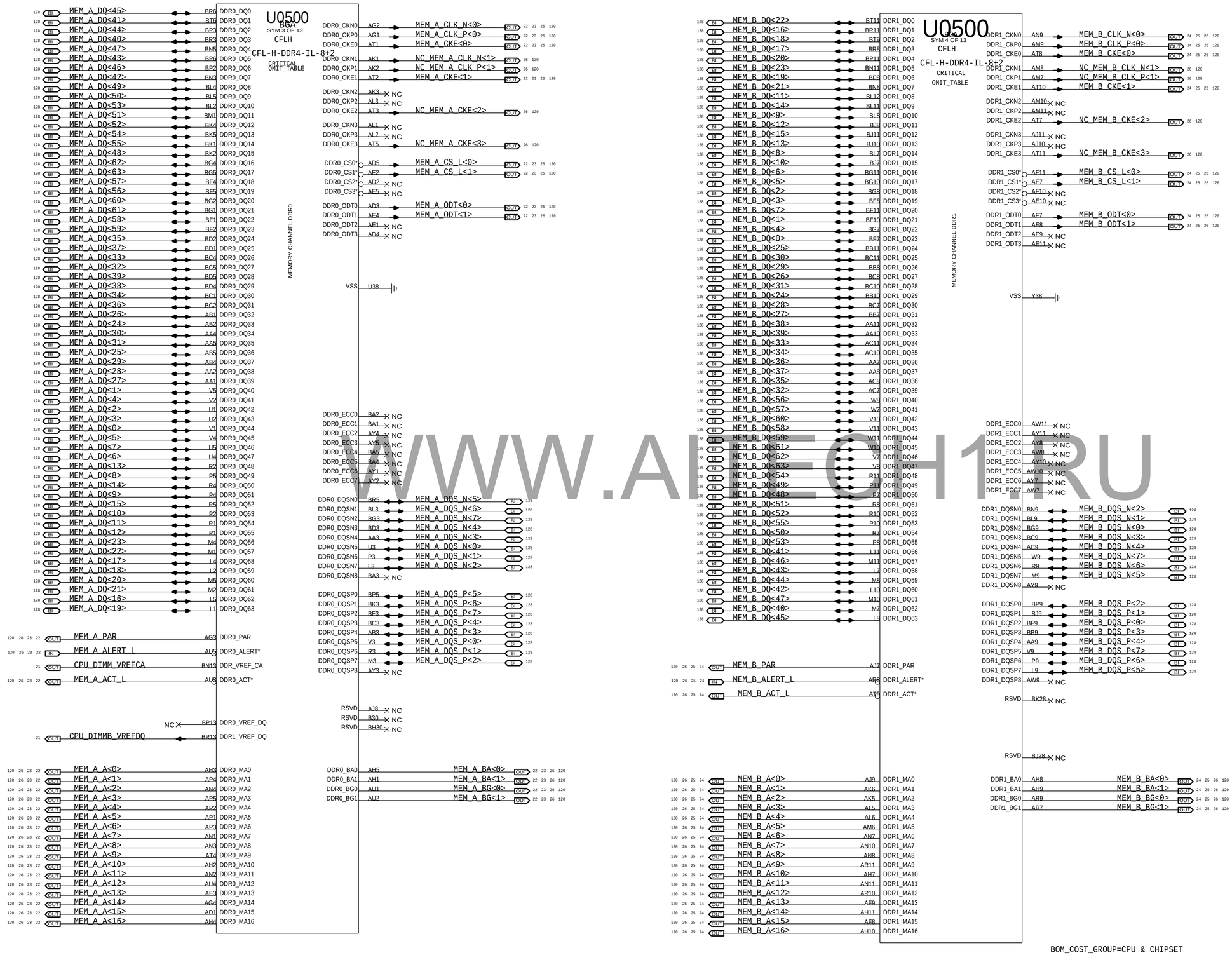

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CPU DDR4 Interfaces

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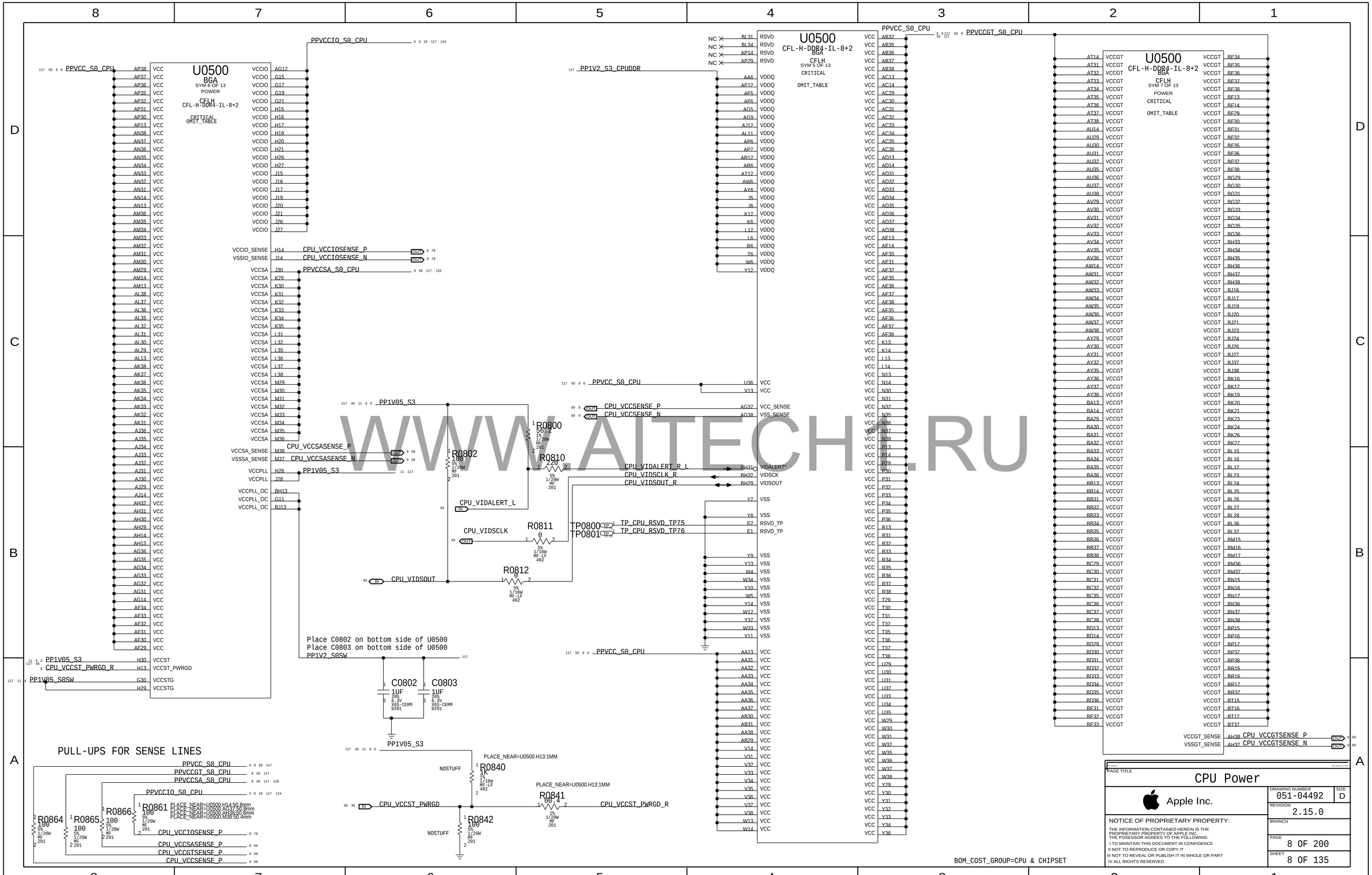

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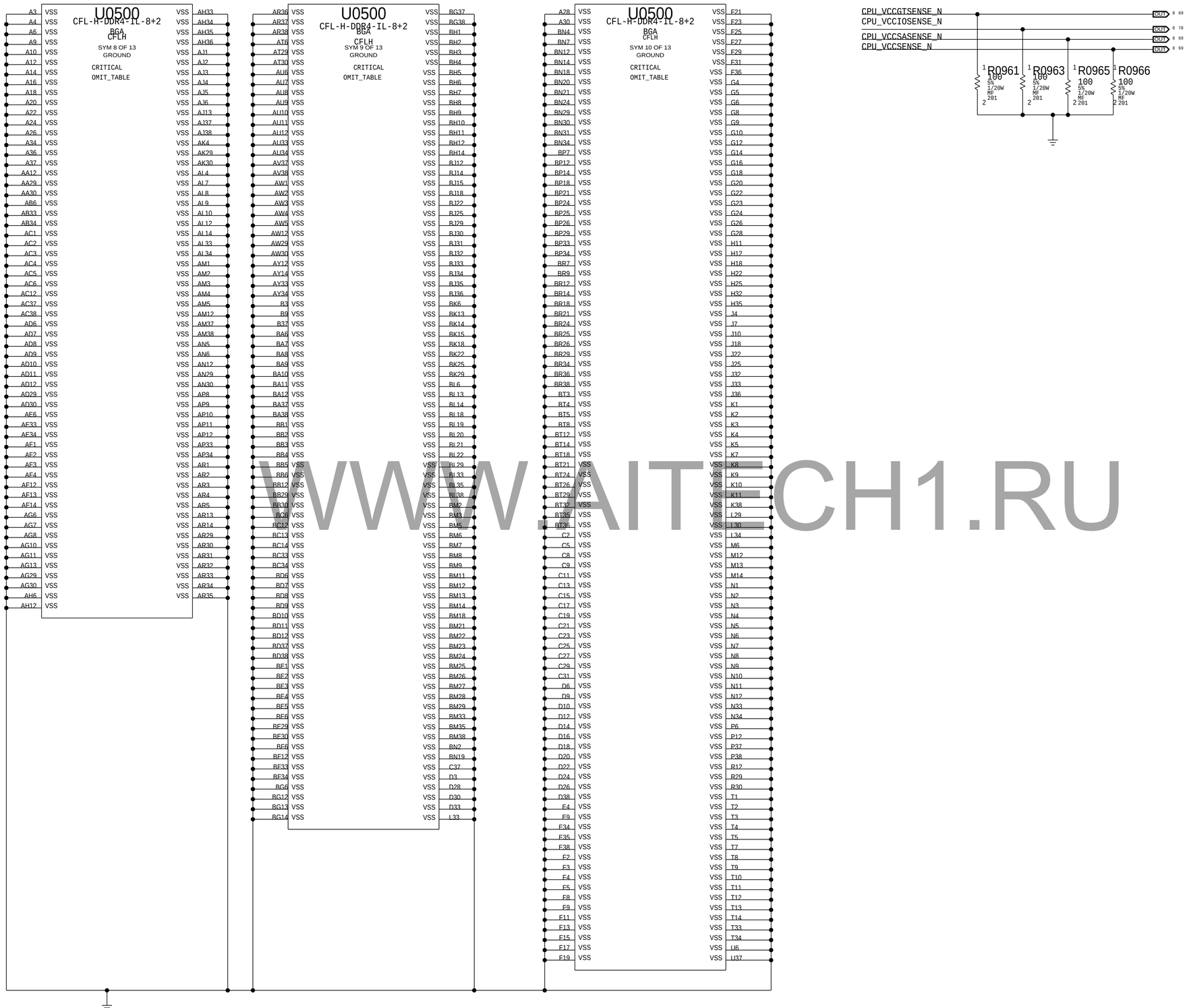

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PAGE TITLE
CPU Ground

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Vcc CPU Core Decoupling from 20140905 BOM

CPU VCORE Decoupling

Intel recommendation: 5x 220uF ESR 5m ohms ESL 1.9nH each,4x 47uF 0805 8x22uF 0603, 28x 10uF 0402, 3x 10uF 0402, 69x 1uF 0201 Board Edge: 2x 220uF, 4x 47uF rest on the back side
Apple Implementation:

126 117 PPVCC_S0_CPU

Place on bottom side of U0500

C1000 C1001 C1002 C1003 C1004 C1005 C1006 C1007 C1008 C1009 C1010 C1011 C1012 C1013 C1014 C1015 C1016 C1017 C1018 C1019 C1020 C1021 C1022
1UF 20% 4V CERM-X6S 0201

Place on bottom side of U0500

C1023 C1024 C1025 C1026 C1027 C1028 C1029 C1030 C1031 C1032 C1033 C1034 C1035 C1036 C1037 C1038 C1039 C1040 C1041 C1042 C1043 C1044 C1045
1UF 20% 4V CERM-X6S 0201

Place on bottom side of U0500

C1046 C1047 C1048 C1049 C1050 C1051 C1052 C1053 C1054 C1055 C1056 C1057 C1058 C1059 C1060 C1061 C1062
1UF 20% 4V CERM-X6S 0201

Place near inductors on bottom side.

C10A0 C10A3 C10A4 C10Z4 C10A6 C10A7 C10A8 C10ZB C10B0 C10B1 C10B4 C10C0 C10C1 C10C4 C10C5 C10C6 C10C7
20UF 20% 2.5V X6S-CERM 0402-1

Noise Floor caps

C10D1 C10D2 C10D3 C10D4 C10D5 C10D6 C10E2 C10E3 C10N1 C10N2 C10N3 C10N4 C10N5 C10N6 C10N7
20UF 20% 2.5V X6S-CERM 0402-1; 12PF 5% 25V NP0-C0G 0201

C10F0 C10F1 C10F2 C10F3 C10F4 C10F5 C10F6 C10F7 C10F8 C10F9 C10G0
20UF 20% 2.5V X6S-CERM 0402-1

CRITICAL C1069 C1068 C1070 C1072 C1073
220UF 20% 2V ELEC SM

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125 124 117 PP1V2_S3_CPUDDR

Place on bottom side of U0500.

C1080 C1081 C1082 C1083 C1084 C1085
20UF 20% 2.5V X6S-CERM 0402-1

CPU VDDQ Decoupling

Intel recommendation: 10x 10uF 0402, 4x 22uF 0602
Apple Implementation:

Place on bottom side of U0500

C1090 C1091 C1092 C1093 C1094 C1095
20UF 20% 2.5V X6S-CERM 0402-1

CRITICAL C1096
220UF 20% 2V ELEC SM

CPU VCCIO Decoupling

Intel recommendation: 3x 10uF 0402 (opposite CPU)
Apple Implementation:

Place near U0500 on bottom side

124 117 8 5 PPVCCIO_S0_CPU

C1086 C1087 C1088 C1089 C108A C108B C108C C108D
20UF 20% 2.5V X6S-CERM 0402-1

NOTE: Intel decoupling recommendations from CBR schematics for Skylake H doc#557227 and PDG section 48.1 (document# 546884)

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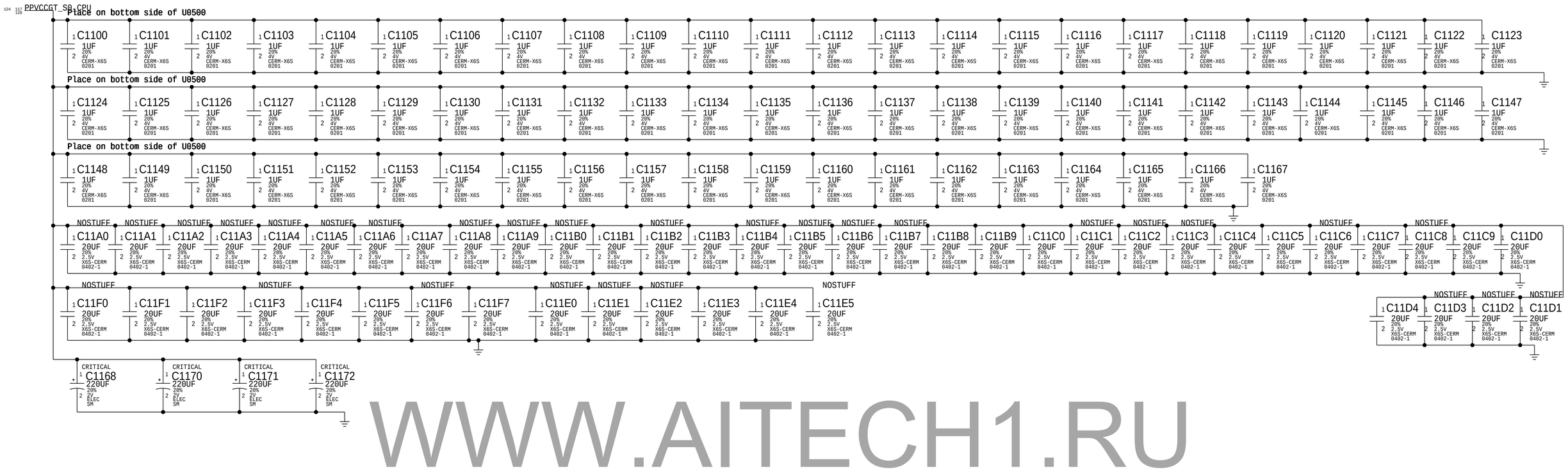
Vcc GT Slice Core Decoupling from 20140905 BOM

CPU VGTSlice Decoupling

Intel recommendation: 7x 220uF, 6x 47uF 0805, 6x 22uF 0603, 35x 10uF 0402, 68 1uF 0201
Apple Implementation:

Board Edge: 4x220uF, 7x 47uF rest on back side



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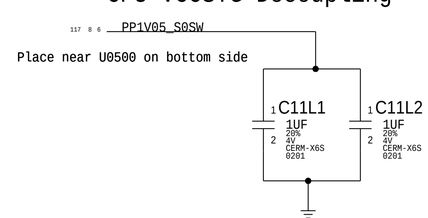
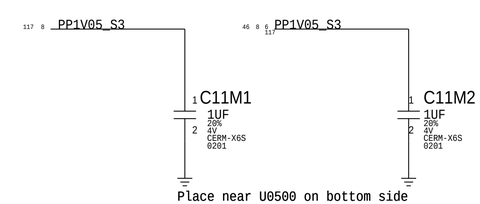
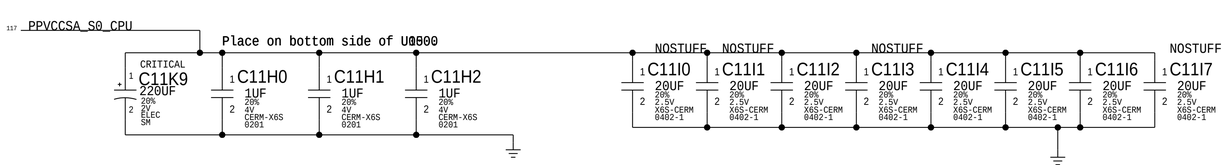
CPU VCCSTG Decoupling



CPU VCCPLL and VCCST Decoupling





CPU VCCSA Decoupling

Intel recommendation: 2x 220uF, 1x 47uF 0805. 1x 22uF. 7x 10uF 0402, 3x 1uF 0201_
2x 220uF, 1x 22uF on board edge, everything else on back side
Apple Implementation:

NOTE: Intel decoupling recommendations from CBR schematics for Skylake H doc#557227 and PDG section 48.1 (document# 546884)

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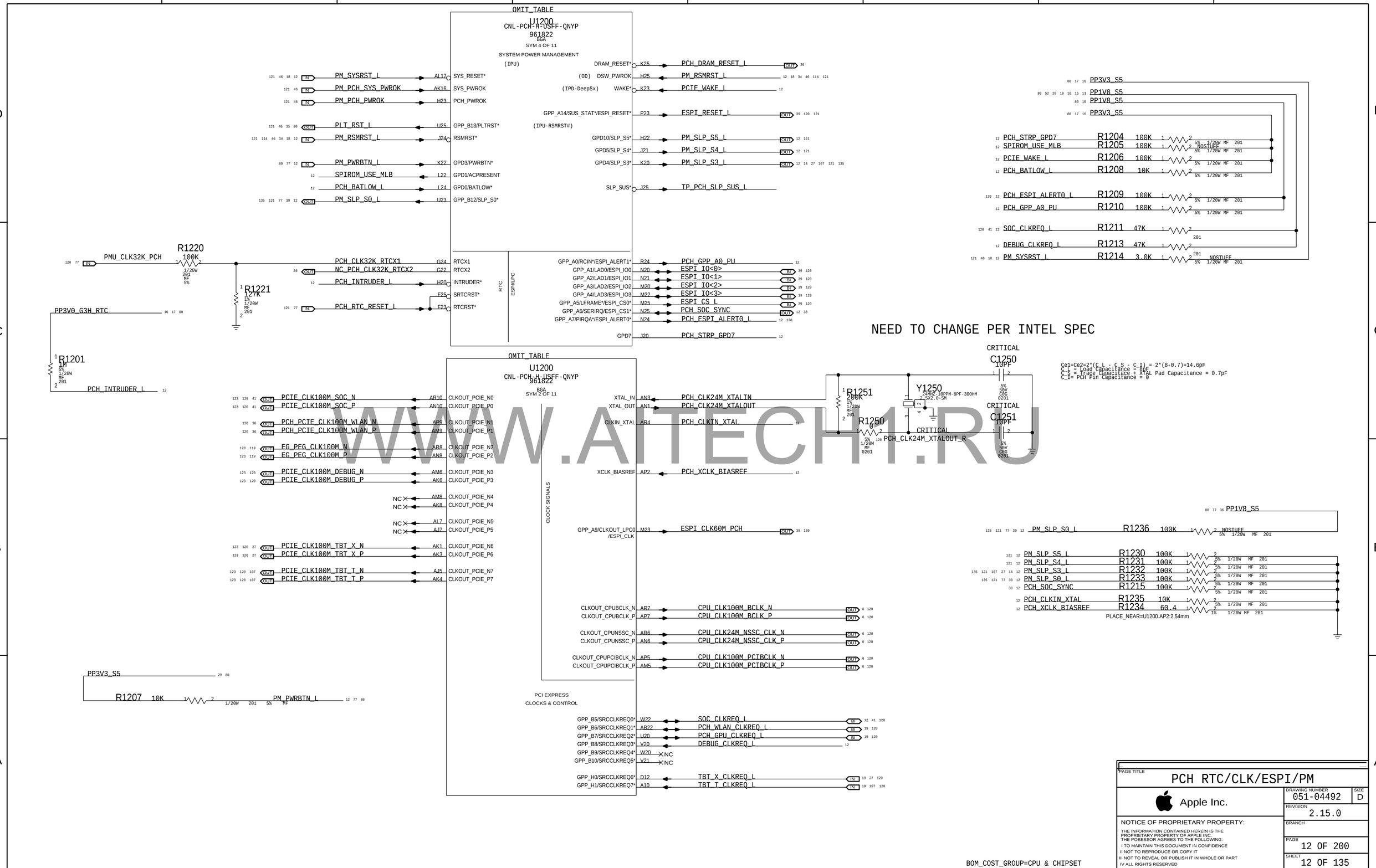

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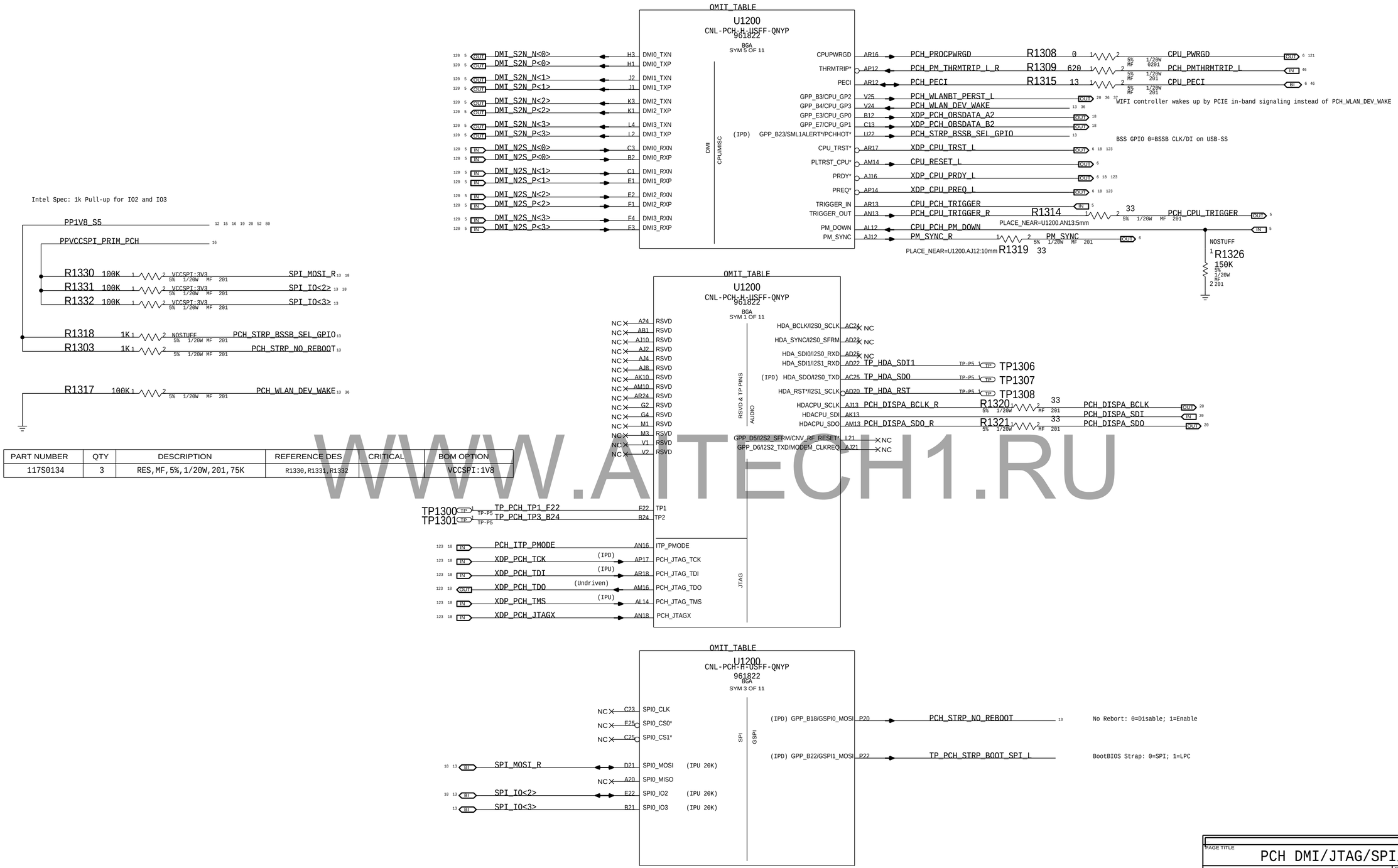

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0134	3	RES,MF,5%,1/20W,201,75K	R1330,R1331,R1332		VCCSPI:1V8

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PCH DMI/JTAG/SPI/HDA

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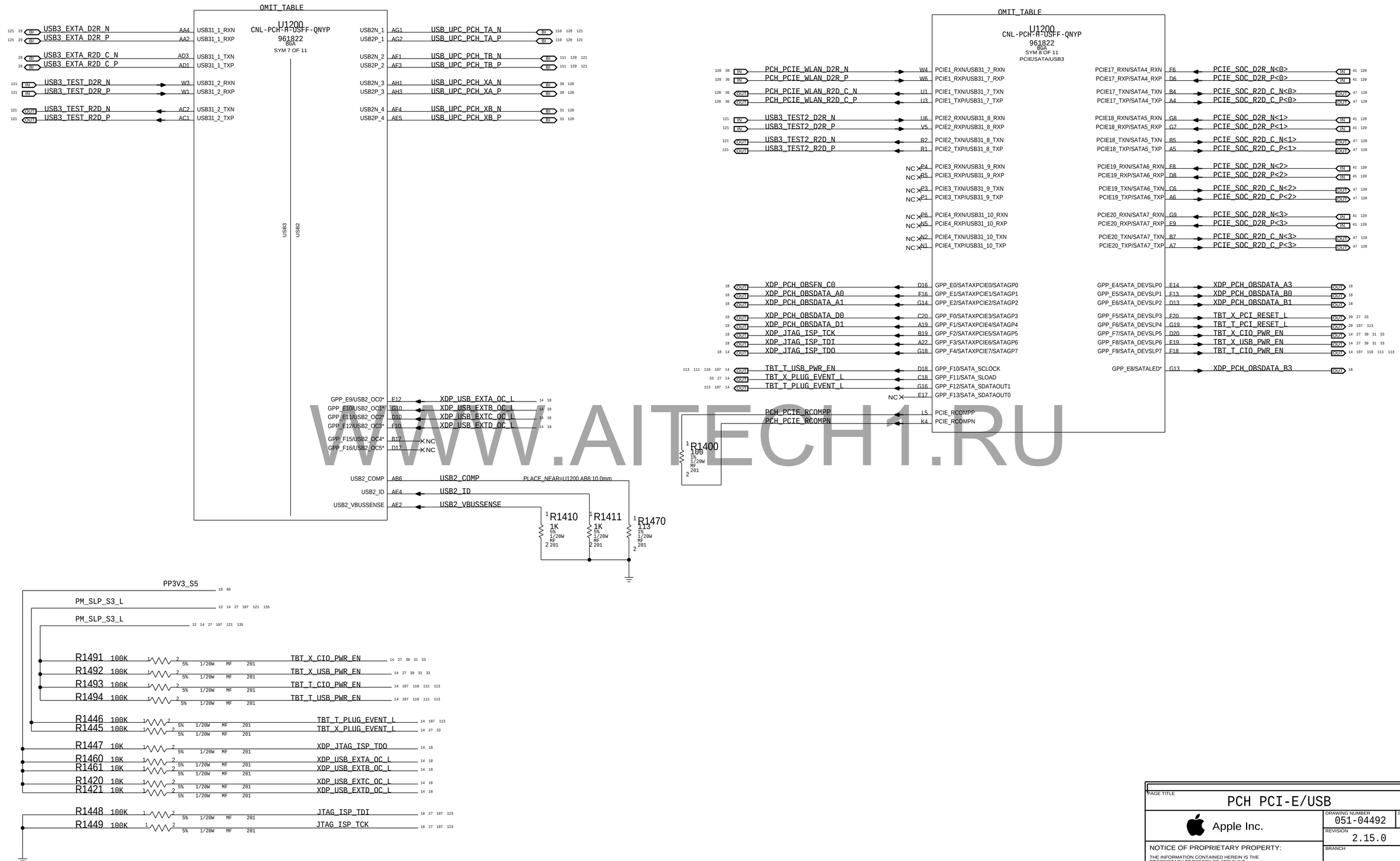

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PCH PCI-E/USB

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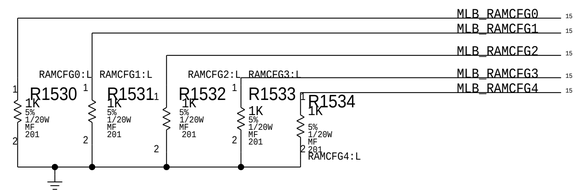
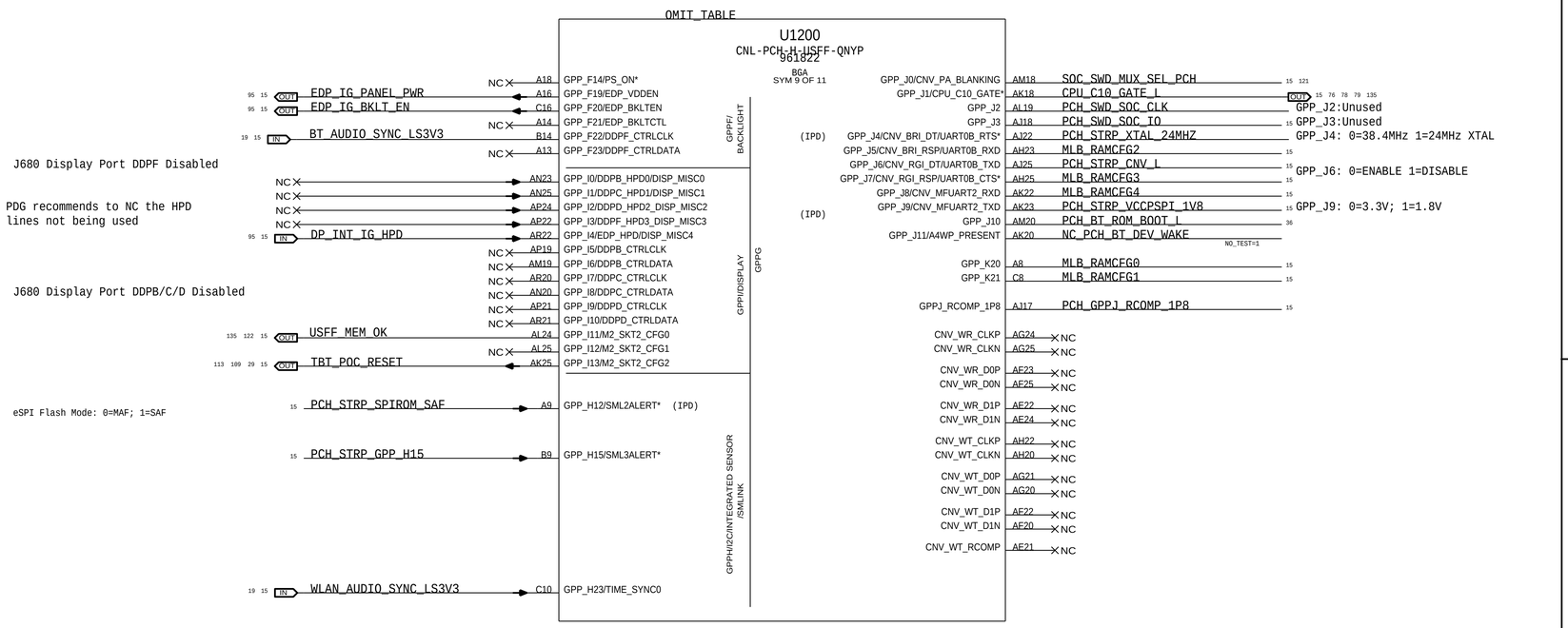
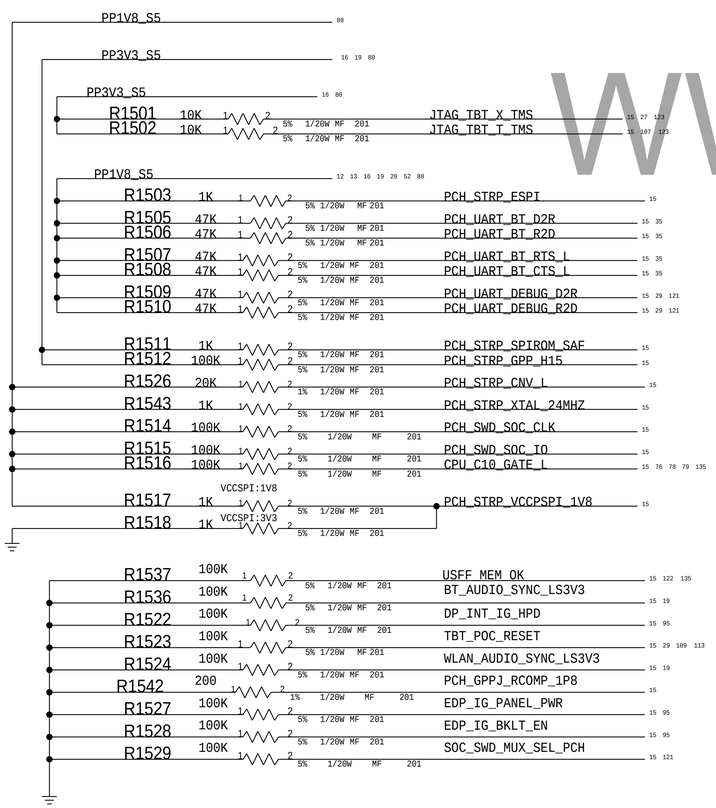
SPEED	CONGIF4
2400MHZ	0
2667MHZ	1

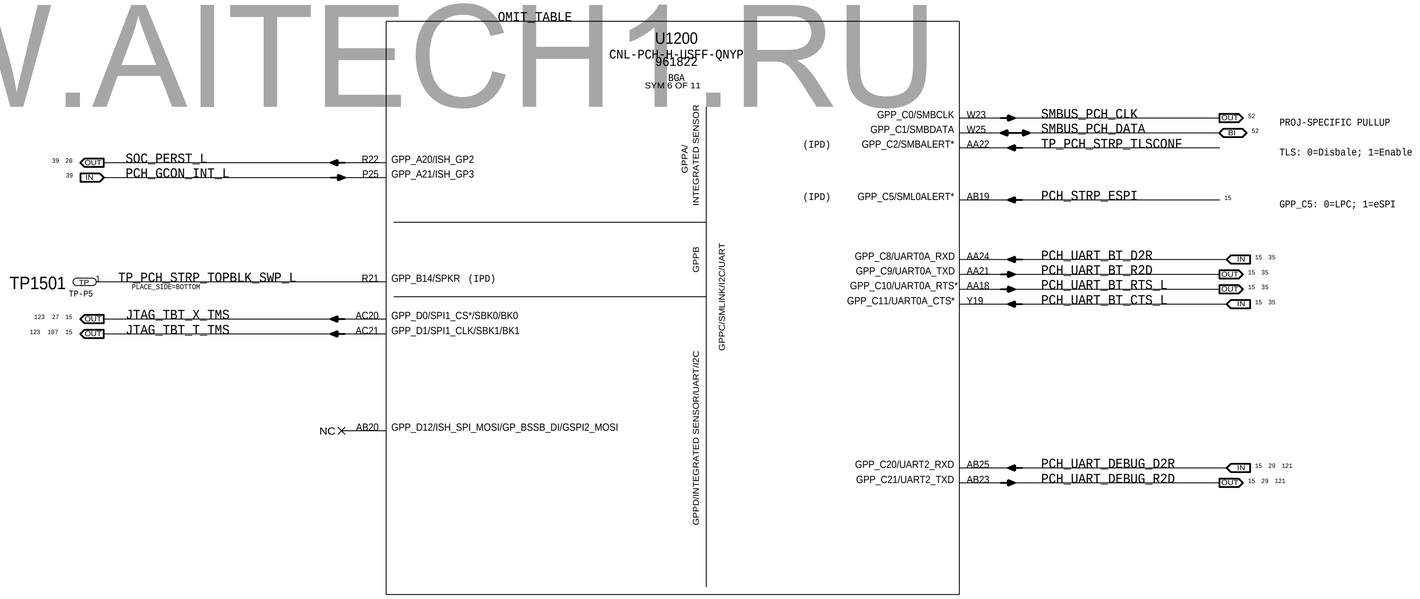
STORAGE	CONGIF3	CONGIF2
16GB	1	1
32GB	0	1
64GB	1	0

VENDOR	CONGIF1	CONGIF0
SAMSUNG	1	1
MICRON	0	1
HYNIX	1	0









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PCH GPIO/MISC/NCTF

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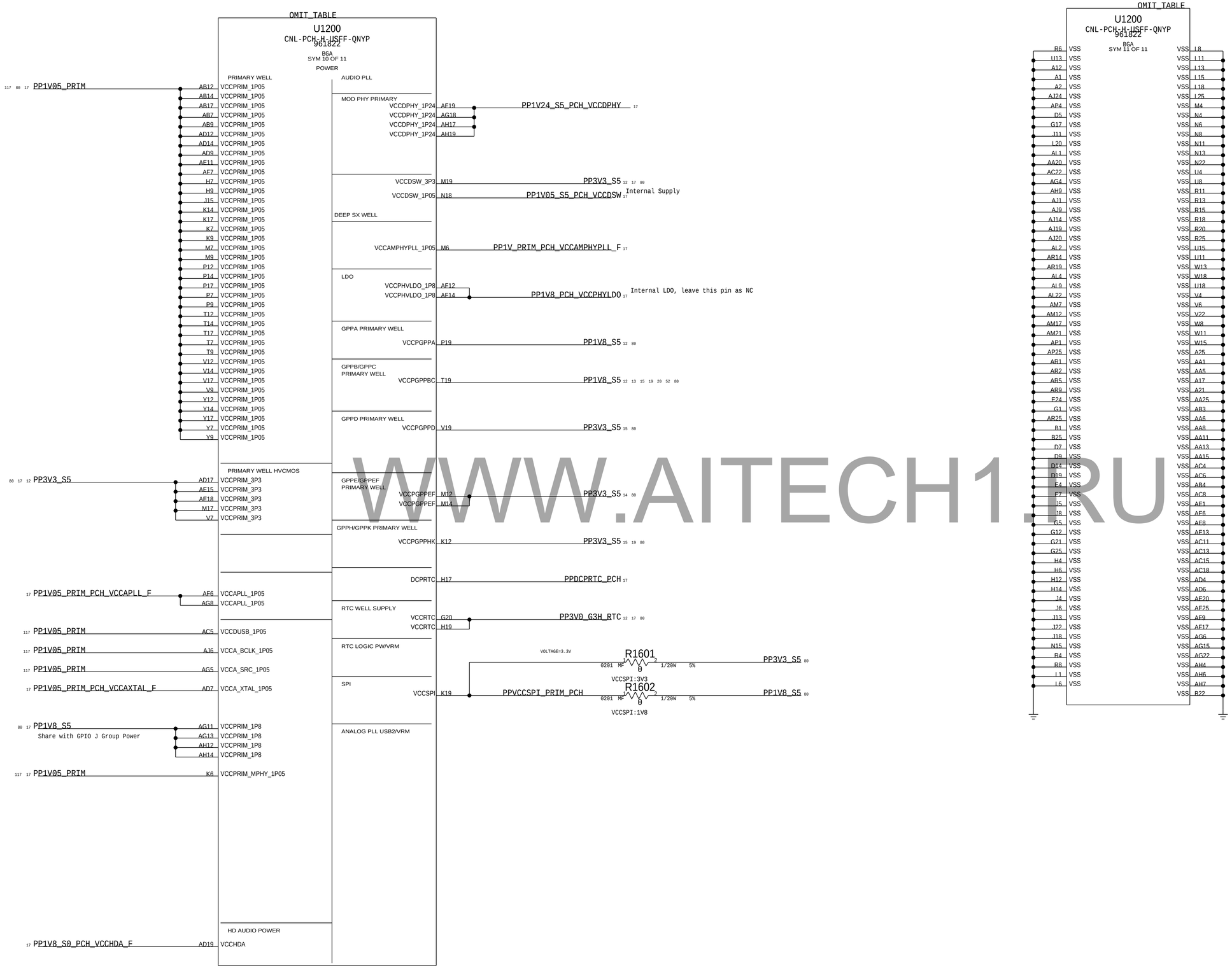

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Current data from LPT EDS (doc #486708, Rev 1.0).

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PCH Power

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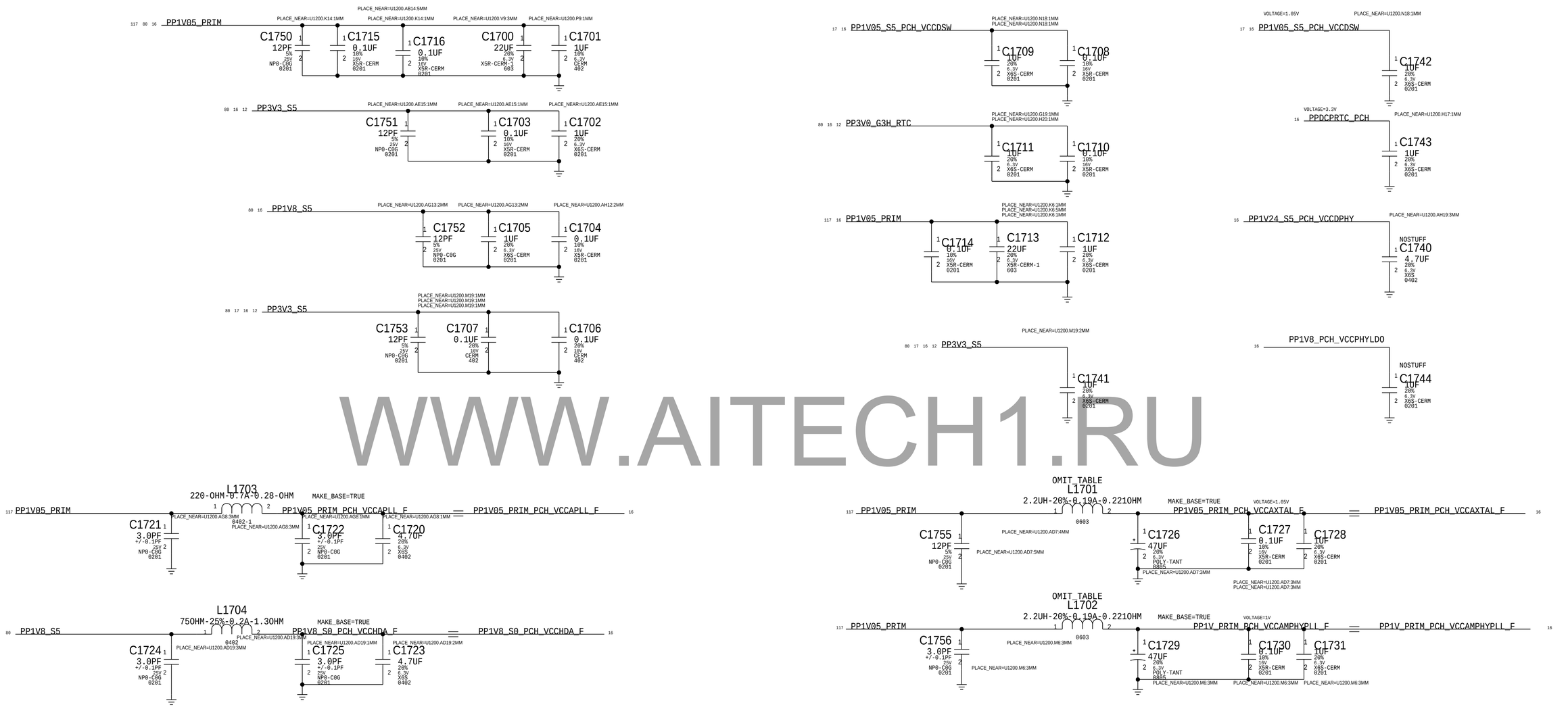

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	2	RES,MF,1A MAX,00HM,5%,0603	L1701,L1702		

Current data from LPT EDS (doc #486708, Rev 1.0).

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: PCH Decoupling

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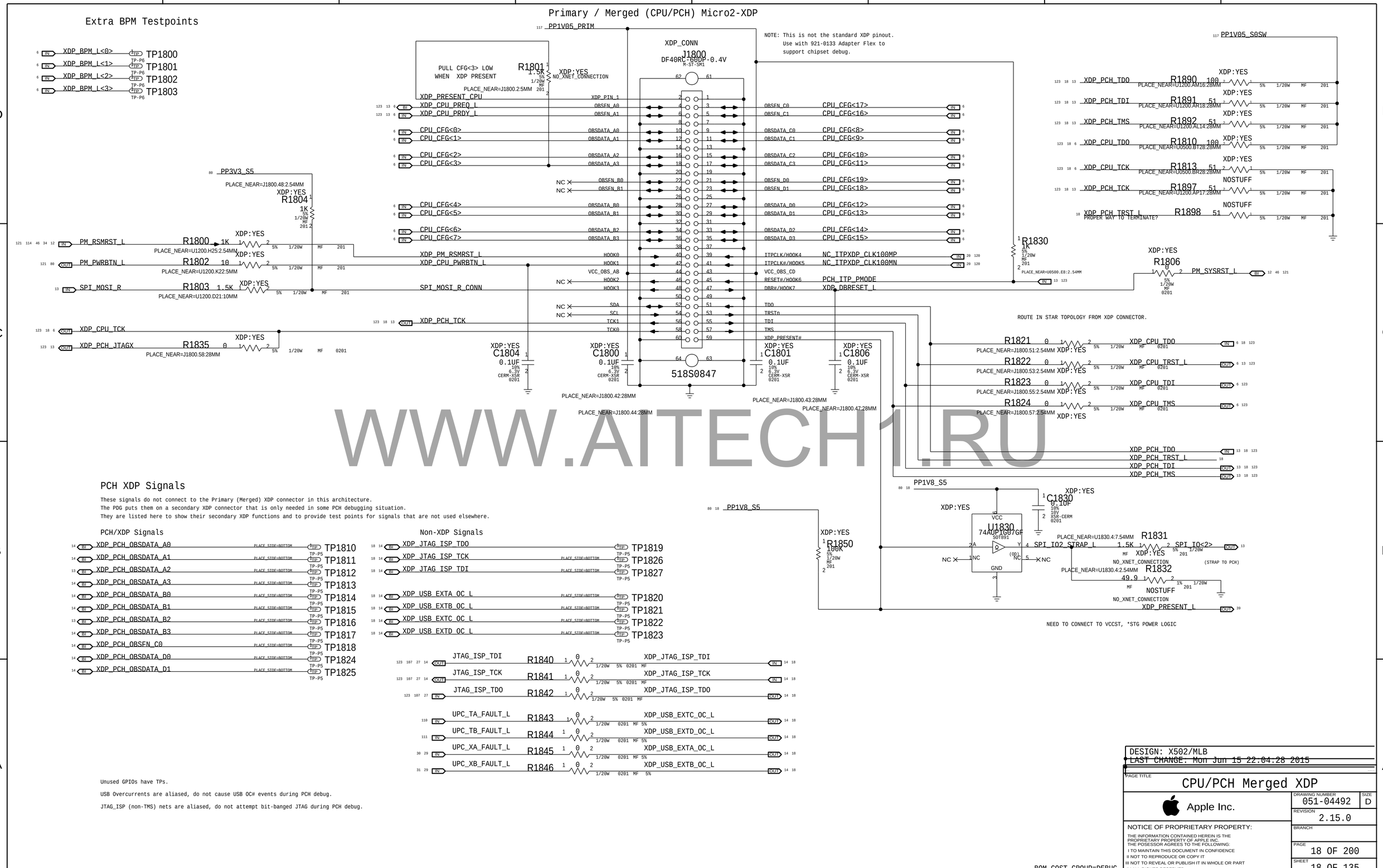

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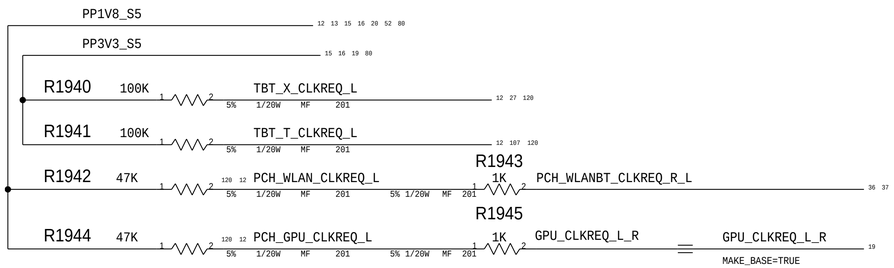
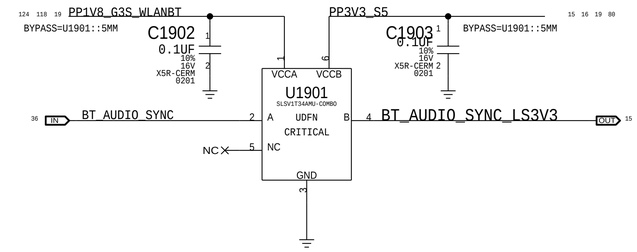
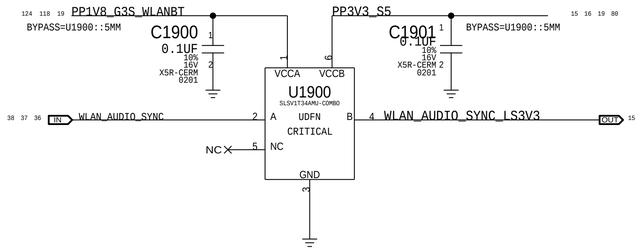
PCIE CLKREQS







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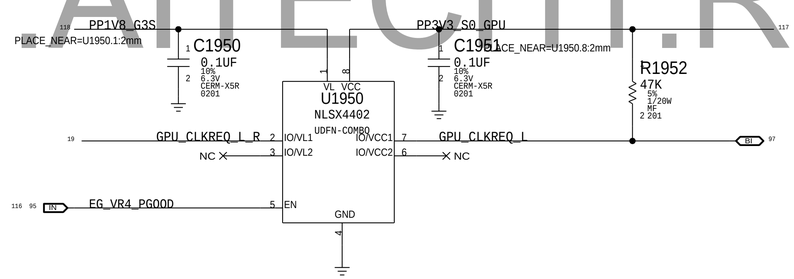

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
Chipset Support 1

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NC ALIASES 3

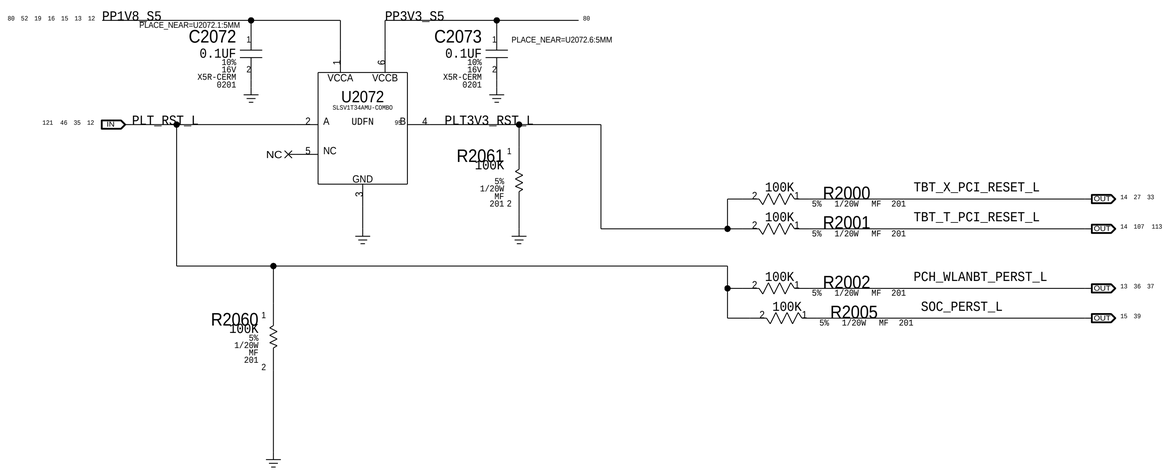
12 NC_PCH_CLK32K_RTCX2 — MAKE_BASE=TRUE — NC_PCH_CLK32K_RTCX2

SIGNAL ALIASES

13 PCH_DISPA_BCLK — MAKE_BASE=TRUE — PCH_DISPA_BCLK 5
13 PCH_DISPA_SDI — MAKE_BASE=TRUE — PCH_DISPA_SDI 5
13 PCH_DISPA_SDO — MAKE_BASE=TRUE — PCH_DISPA_SDO 5

120 18 NC_ITPXDP_CLK100MN — TRUE — NC_ITPXDP_CLK100MN
120 18 NC_ITPXDP_CLK100MP — TRUE — NC_ITPXDP_CLK100MP

Platform Reset Connections



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BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
Chipset Support 2

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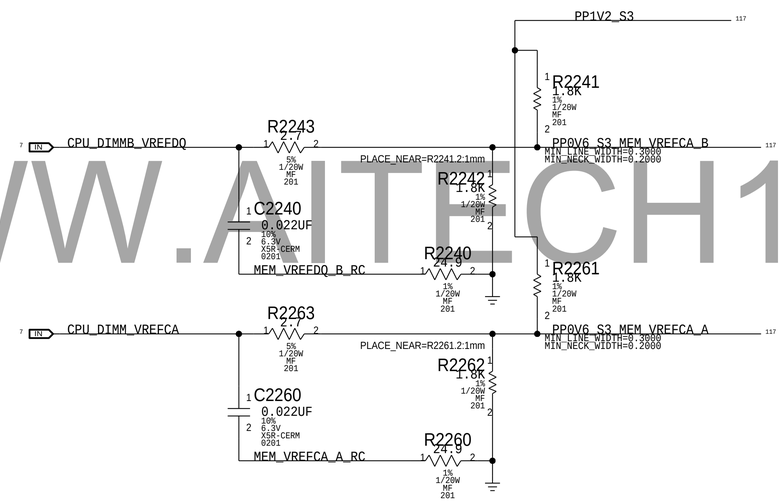
CPU-Based Margining
VRef Dividers

```
DDR4 VDDQ = 1.2V
-----------------
MIMINUM Step Size = 0.50% * VDDQ = 6.0mV per step
TYPICAL Step Size = 0.65% * VDDQ = 7.8mV per step
MAXIMUM Step Size = 0.80% * VDDQ = 9.6mV per step

 KBL PLATFORM GUIDE Page.102 FOR DDR4 X8 MEMORY DOWN
 ---------------------------------------------------
 DDR0_VREF_DQ = Not Used
 DDR1_VREF_DQ = Reference For Channel B
 DDR_VREF_CA = Reference For Channel A
```



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BOM_COST_GROUP=DRAM

PAGE TITLE	DDR4 VREF Margining
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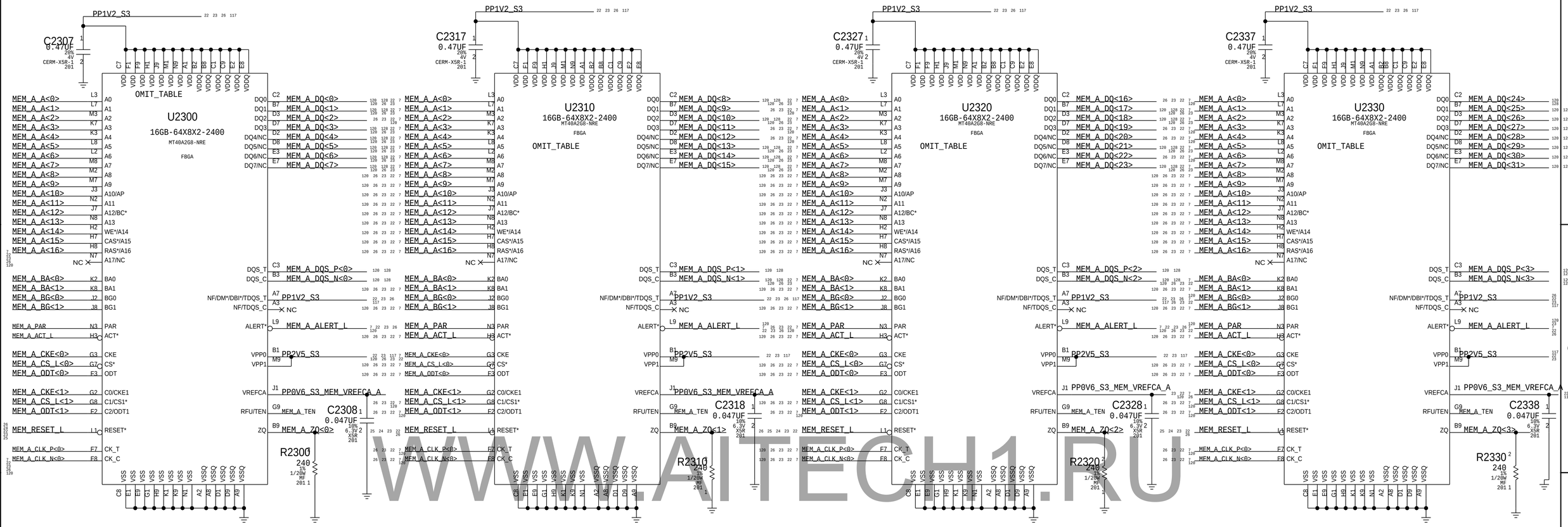

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PAGE TITLE
DDR4 SDRAM Channel A 1

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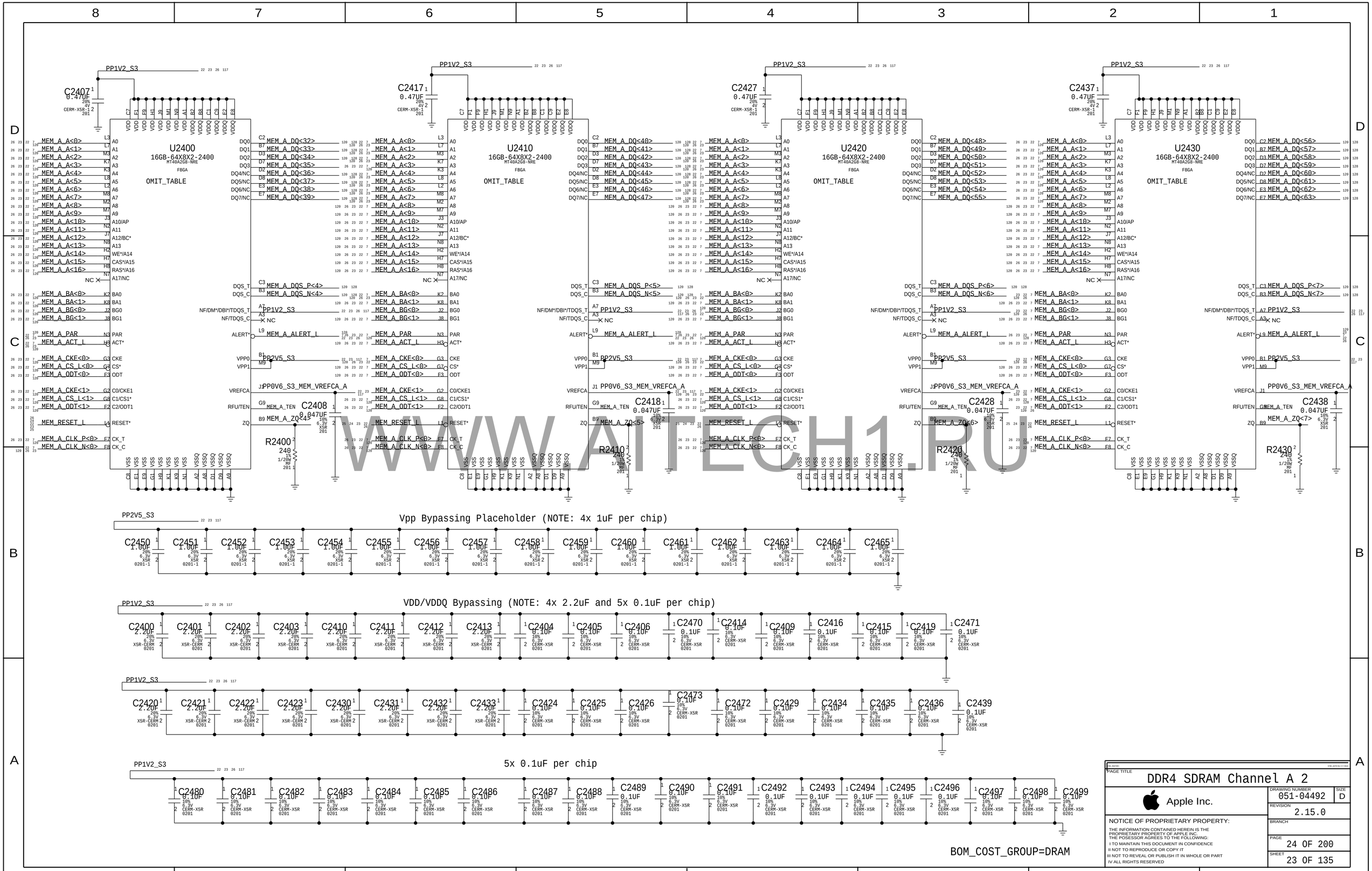

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DDR4 SDRAM Channel A 2

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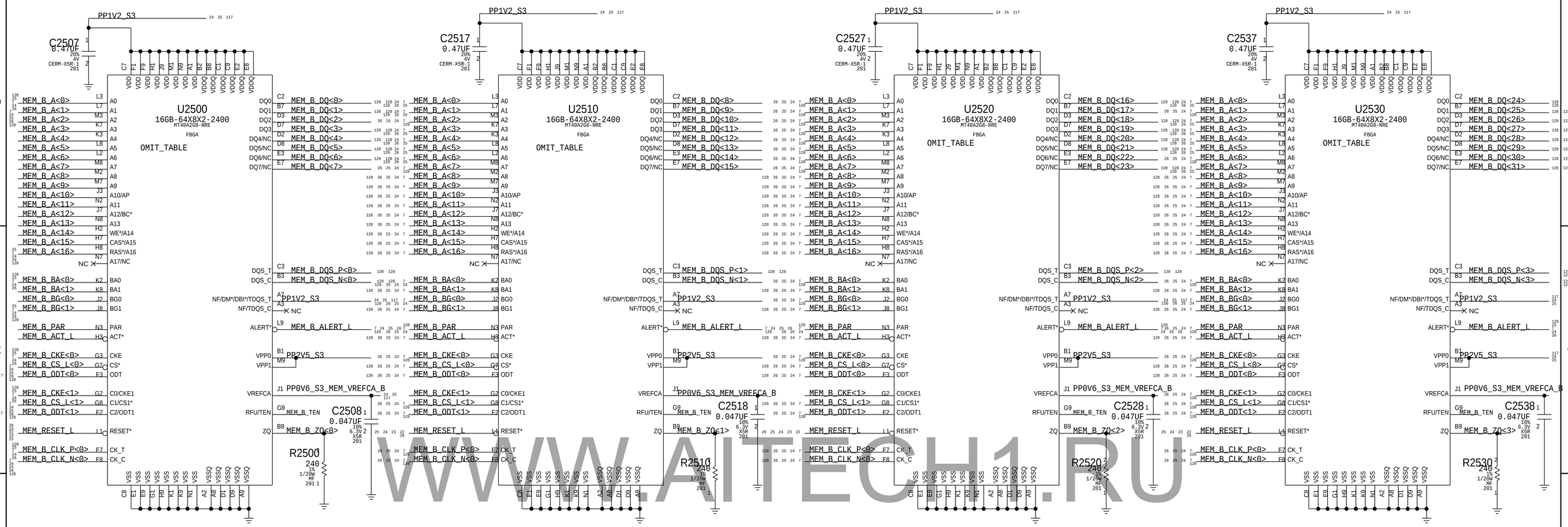
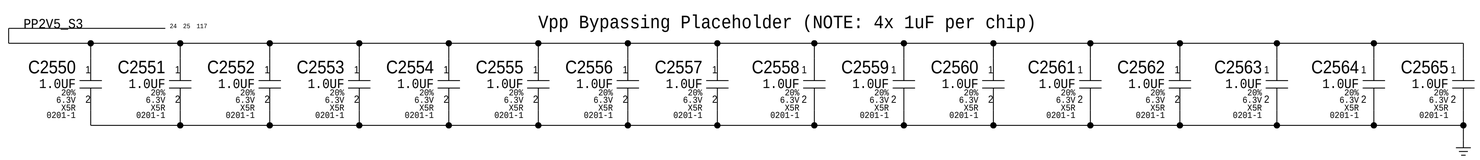
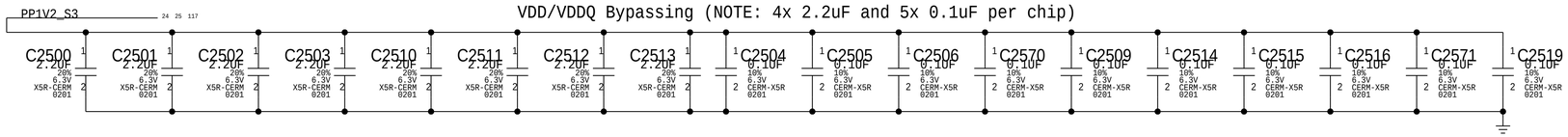


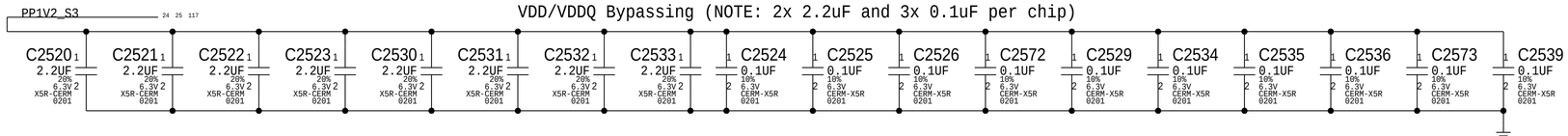
Vpp Bypassing Placeholder (NOTE: 4x 1uF per chip)



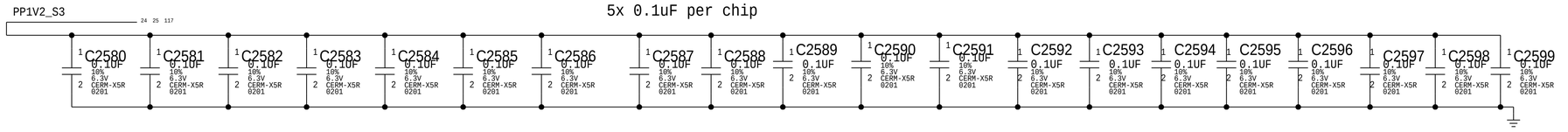
VDD/VDDQ Bypassing (NOTE: 4x 2.2uF and 5x 0.1uF per chip)



VDD/VDDQ Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)



5x 0.1uF per chip



BOM_COST_GROUP=DRAM

PAGE TITLE: DDR4 SDRAM Channel B 1

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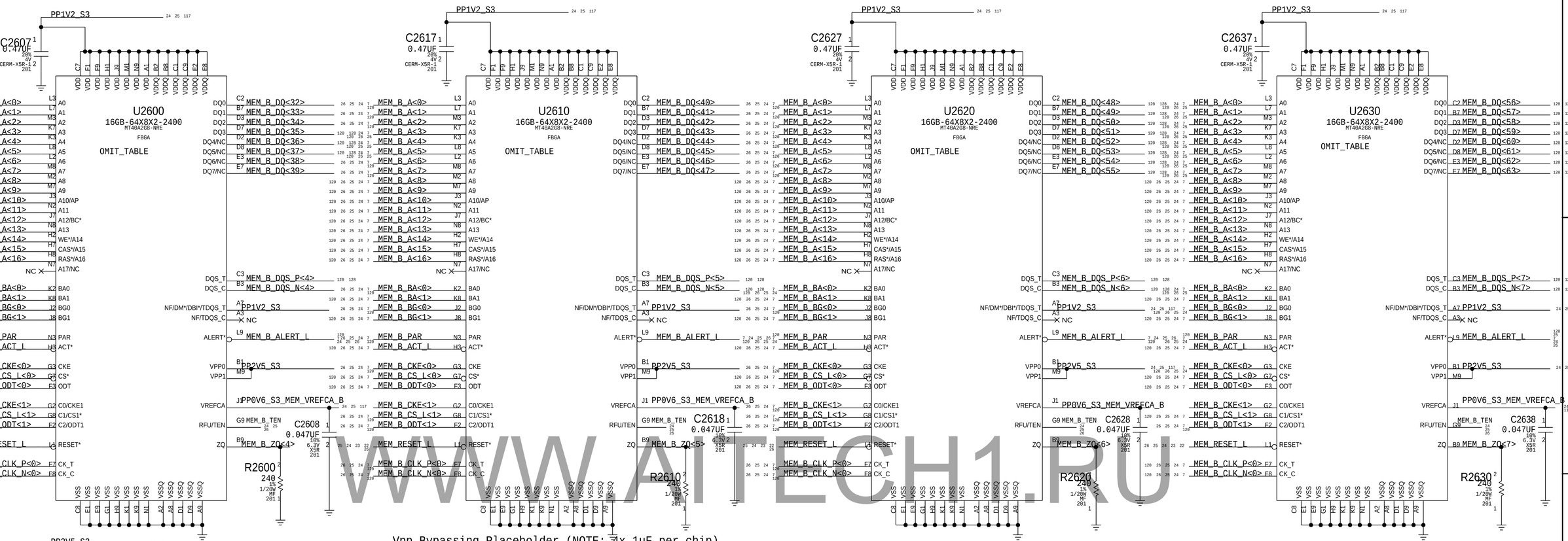

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JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE

PP0V6_S0_DDRVTT

C2701,C2721 FOR DESENSE IMPROVEMENT
LOCATION DEPENDS ON DESENSE TEAM

MEM_A_A<0>	R2700	36	C2700 2.2UF 20% 4V X5R-CERM 0201	C2701 12PF 5% NPO-C0G 0201 25V
MEM_A_A<1>	R2701	36		
MEM_A_A<2>	R2702	36		
MEM_A_A<3>	R2703	36		
MEM_A_A<4>	R2704	36	C2702 2.2UF 20% 4V X5R-CERM 0201	C2703 2.2UF 20% 4V X5R-CERM 0201
MEM_A_A<5>	R2705	36		
MEM_A_A<6>	R2706	36		
MEM_A_A<7>	R2707	36		
MEM_A_A<8>	R2708	36	C2704 2.2UF 20% 4V X5R-CERM 0201	C2705 0.47UF 20% 4V CERM-X5R-1 201
MEM_A_A<9>	R2709	36		
MEM_A_A<10>	R2710	36		
MEM_A_A<11>	R2711	36		
MEM_A_A<12>	R2712	36	C2706 0.47UF 20% 4V CERM-X5R-1 201	C2707 0.47UF 20% 4V CERM-X5R-1 201
MEM_A_A<13>	R2713	36		
MEM_A_A<14>	R2714	36		
MEM_A_A<15>	R2715	36		
MEM_A_A<16>	R2716	36	C2708 0.47UF 20% 4V CERM-X5R-1 201	C2711 2.2UF 20% 4V X5R-CERM 0201
MEM_A_BA<0>	R2717	36		
MEM_A_BA<1>	R2718	36		
MEM_A_BG<0>	R2719	36		
MEM_A_BG<1>	R2720	36	C2710 0.47UF 20% 4V CERM-X5R-1 201	C2712 2.2UF 20% 4V X5R-CERM 0201
MEM_A_CS_L<0>	R2721	36		
MEM_A_CS_L<1>	R2722	36		
MEM_A_CKE<0>	R2723	36		
MEM_A_CKE<1>	R2724	36		
MEM_A_ODT<0>	R2725	36		
MEM_A_ODT<1>	R2726	36		
MEM_A_ACT_L	R2727	36		
MEM_A_PAR	R2728	36		

PP0V6_S0_DDRVTT

MEM_B_A<0>	R2770	36	C2720 2.2UF 20% 4V X5R-CERM 0201	C2721 12PF 5% NPO-C0G 0201 25V
MEM_B_A<1>	R2771	36		
MEM_B_A<2>	R2772	36		
MEM_B_A<3>	R2773	36		
MEM_B_A<4>	R2774	36	C2722 2.2UF 20% 4V X5R-CERM 0201	C2723 2.2UF 20% 4V X5R-CERM 0201
MEM_B_A<5>	R2775	36		
MEM_B_A<6>	R2776	36		
MEM_B_A<7>	R2777	36		
MEM_B_A<8>	R2778	36	C2724 2.2UF 20% 4V X5R-CERM 0201	C2725 0.47UF 20% 4V CERM-X5R-1 201
MEM_B_A<9>	R2779	36		
MEM_B_A<10>	R2780	36		
MEM_B_A<11>	R2781	36		
MEM_B_A<12>	R2782	36	C2726 0.47UF 20% 4V CERM-X5R-1 201	C2727 0.47UF 20% 4V CERM-X5R-1 201
MEM_B_A<13>	R2783	36		
MEM_B_A<14>	R2784	36		
MEM_B_A<15>	R2785	36		
MEM_B_A<16>	R2786	36	C2728 0.47UF 20% 4V CERM-X5R-1 201	C2734 2.2UF 20% 4V X5R-CERM 0201
MEM_B_BA<0>	R2787	36		
MEM_B_BA<1>	R2788	36		
MEM_B_BG<0>	R2789	36		
MEM_B_BG<1>	R2790	36	C2730 0.47UF 20% 4V CERM-X5R-1 201	C2735 2.2UF 20% 4V X5R-CERM 0201
MEM_B_CS_L<0>	R2791	36		
MEM_B_CS_L<1>	R2792	36		
MEM_B_CKE<0>	R2793	36		
MEM_B_CKE<1>	R2794	36		
MEM_B_ODT<0>	R2795	36		
MEM_B_ODT<1>	R2796	36		
MEM_B_ACT_L	R2797	36		
MEM_B_PAR	R2798	36		

MEM_A_TEN — R2752 0 5% 1/20W MF 0201 — MEM_A_TEN_R — TP2700 TP-P5
R2753 100 5% 1/20W MF 201; NOSTUFF C2752 0.47UF 20% 4V CERM-X5R-1 201

MEM_B_TEN — R2754 0 5% 1/20W MF 0201 — MEM_B_TEN_R — TP2701 TP-P5
R2755 100 5% 1/20W MF 201; NOSTUFF C2753 0.47UF 20% 4V CERM-X5R-1 201

MEM Clock Termination

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM

MEM_A_CLK_N<0> — PLACE_NEAR=U2430.F8:8mm — R2750 30 5% 1/20W MF 201 — MEM_A_CLK0_TERM_R — C2751 0.01UF 10% 25V X5R-CERM 0201 — PP0V6_S0_DDRVTT
C2750 3300PF 10% 10V X7R-CERM 0201; NOSTUFF; PLACE_NEAR=U2430.F8:10mm
MEM_A_CLK_P<0> — PLACE_NEAR=U2430.F7:8mm — R2751 30 5% 1/20W MF 201

MEM_B_CLK_N<0> — PLACE_NEAR=U2630.F8:8mm — R2760 30 5% 1/20W MF 201 — MEM_B_CLK0_TERM_R — C2761 0.01UF 10% 25V X5R-CERM 0201 — PP0V6_S0_DDRVTT
C2760 3300PF 10% 10V X7R-CERM 0201; NOSTUFF; PLACE_NEAR=U2630.F8:10mm
MEM_B_CLK_P<0> — PLACE_NEAR=U2630.F7:8mm — R2761 30 5% 1/20W MF 201

NC_MEM_A_CLK_N<1>	MAKE_BASE=TRUE	NC_MEM_A_CLK_N<1>
NC_MEM_A_CLK_P<1>	MAKE_BASE=TRUE	NC_MEM_A_CLK_P<1>
NC_MEM_A_CKE<2>	MAKE_BASE=TRUE	NC_MEM_A_CKE<2>
NC_MEM_A_CKE<3>	MAKE_BASE=TRUE	NC_MEM_A_CKE<3>
NC_MEM_B_CLK_N<1>	MAKE_BASE=TRUE	NC_MEM_B_CLK_N<1>
NC_MEM_B_CLK_P<1>	MAKE_BASE=TRUE	NC_MEM_B_CLK_P<1>
NC_MEM_B_CKE<2>	MAKE_BASE=TRUE	NC_MEM_B_CKE<2>
NC_MEM_B_CKE<3>	MAKE_BASE=TRUE	NC_MEM_B_CKE<3>

PP1V2_S3
R2730 51 1% 1/20W MF 201
R2731 51 1% 1/20W MF 201
R2733 470 1% 1/20W MF 201

MEM_A_ALERT_L
MEM_B_ALERT_L
PCH_DRAM_RESET_L — R2732 0 5% 1/20W MF 0201 — MEM_RESET_L — C2732 0.1UF 10% 6.3V CERM-X5R 0201; NOSTUFF

BOM_COST_GROUP=DRAM

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DDR4 Termination

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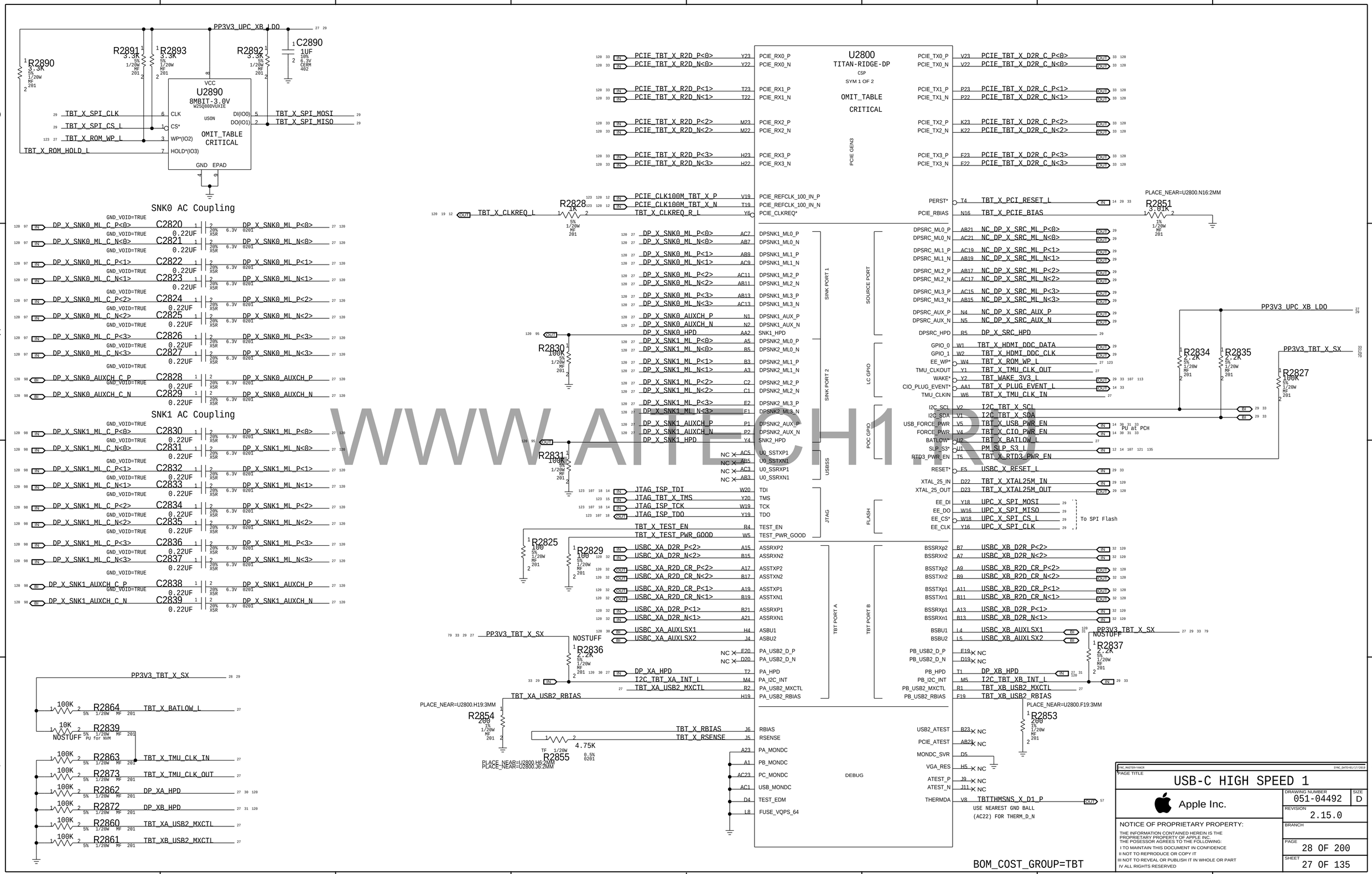

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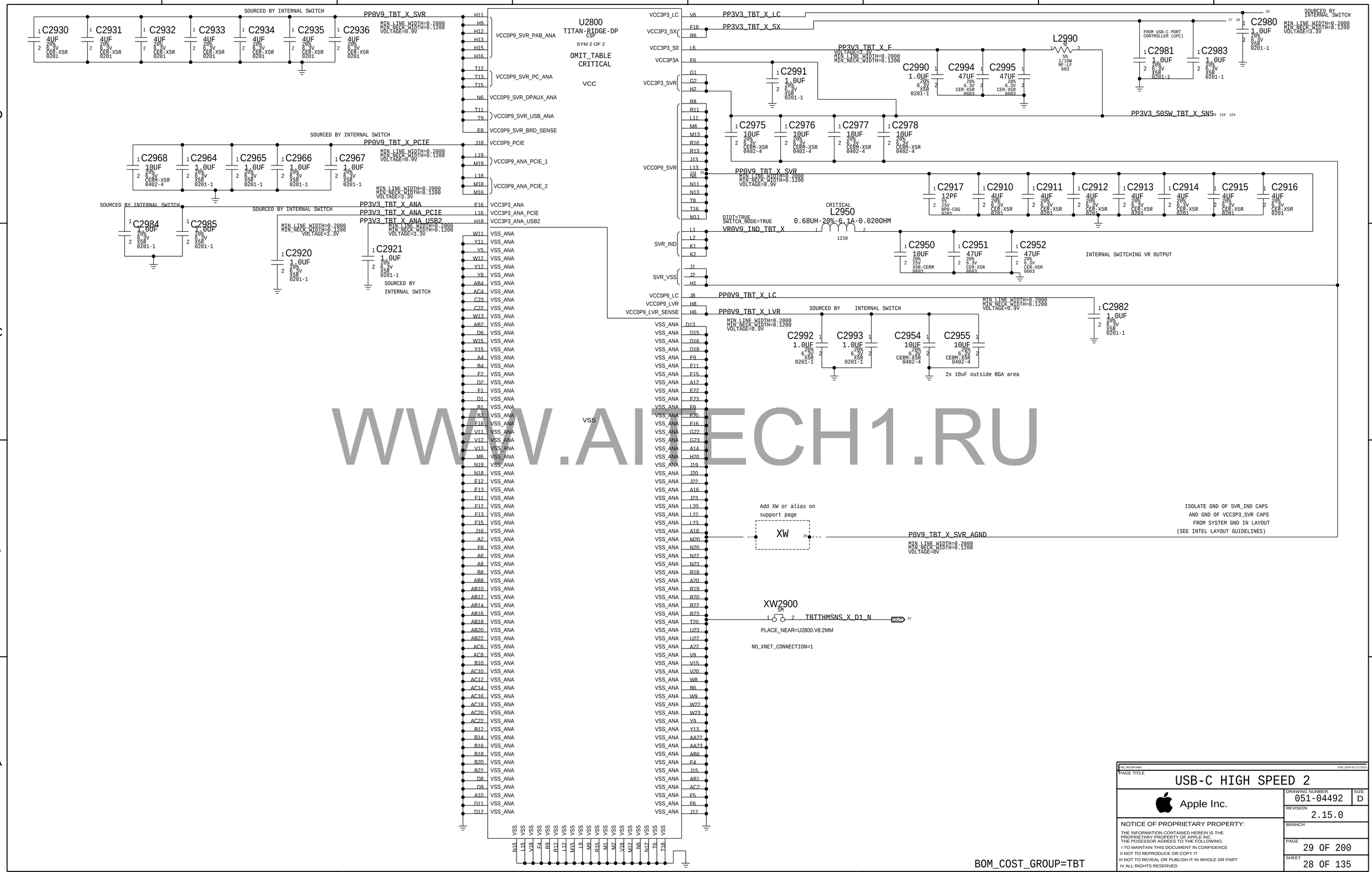

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PAGE TITLE
USB-C HIGH SPEED 2

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TBT WAKE LEVEL SHIFTER

PP3V3_G3H_RTC_X
PP1V8_SLPS2R — Q3001 DMN32D2LFB4 (DFN1006H4-3) — R3003 100K 5% 1/20W MF 201
SMC HAS IPU
TBT_WAKE_L (OUT) — TBT_WAKE_3V3_L (IN)

DP SRC OPTIONS

IF DP SRC NOT USED

DP_X_SRC_HPD — R3017 100K 1/20W 5% MF 201

=DP_X_SRC_ML_P<3..0> — NC_DP_X_SRC_ML_P<3..0> (MAKE_BASE=TRUE, NO_TEST=1)
=DP_X_SRC_ML_N<3..0> — NC_DP_X_SRC_ML_N<3..0> (MAKE_BASE=TRUE, NO_TEST=1)

Bus <3..0> doesn't resolve properly. but netlist is correct.

NC_DP_X_SRC_AUX_P — NC_DP_X_SRC_AUX_P (MAKE_BASE=TRUE, NO_TEST=1)
NC_DP_X_SRC_AUX_N — NC_DP_X_SRC_AUX_N (MAKE_BASE=TRUE, NO_TEST=1)

FUSES FOR UPC

PPDCIN_G3H — F3000 (CRITICAL, 0603-1, 6A-32V) — PPDCIN_XA_G3H_F
PPDCIN_XB_G3H_F — F3001 (CRITICAL, 0603-1, 6A-32V)

Ridge 25MHz xtal

TBT_X_XTAL25M_OUT — C3002 20PF (5% 25V C0G 0201)
Y3000 (CRITICAL) 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM
TBT_X_XTAL25M_IN — C3003 20PF (5% 25V C0G 0201)

DEBUG ALIASES

PCH UART (MOJO)

PCH_UART_DEBUG_R2D — PCH_UART_DEBUG_R2D (MAKE_BASE=TRUE)
PCH_UART_DEBUG_D2R — PCH_UART_DEBUG_D2R (MAKE_BASE=TRUE)

SMC UART

SMC_DEBUGPRT_TX — SMC_DEBUGPRT_TX (MAKE_BASE=TRUE)
SMC_DEBUGPRT_RX — SMC_DEBUGPRT_RX (MAKE_BASE=TRUE)

SOC SWD

SWD_SOC_SWCLK (MAKE_BASE=TRUE) — SWD_SOC_SWCLK
R3036 0 0201 5% 1/20W MF — UPC_XB_DBG4 (PLACE_NEAR=U3100.G2:5mm)
SWD_SOC_SWDIO (MAKE_BASE=TRUE) — SWD_SOC_SWDIO
R3037 0 0201 5% 1/20W MF — UPC_XB_DBG5 (PLACE_NEAR=U3100.G2:5mm)

DCI

USB3_EXTA_D2R_P — USB3_EXTA_D2R_P (MAKE_BASE=TRUE)
USB3_EXTA_D2R_N — USB3_EXTA_D2R_N (MAKE_BASE=TRUE)
USB3_EXTA_R2D_C_P — C3004 0.1UF 10% 16V 0201 X5R-CERM — USB3_EXTA_R2D_P (MAKE_BASE=TRUE)
USB3_EXTA_R2D_C_N — C3005 0.1UF 10% 16V 0201 X5R-CERM — USB3_EXTA_R2D_N (MAKE_BASE=TRUE)

DBG MUX PDs

UPC_XA_DBG_PD — UPC_XA_DBG_PD (MAKE_BASE=TRUE) — R3038 100K 5% 1/20W MF 201
UPC_XA_DBG_PD
UPC_XA_DBG_PD
UPC_XA_DBG_PD

Ridge and ACE PU/PDs

UPC_X_5V_EN — R3001 100K
SPARE_UPC_XA_USB3_RP — R3004 100K
SPARE_UPC_XA_USB3_RN — R3008 100K
SPARE_UPC_XB_USB2_RP — R3009 100K
SPARE_UPC_XB_USB2_RN — R3014 100K
SPARE_UPC_XB_USB3_RP — R3018 100K
SPARE_UPC_XB_USB3_RN — R3020 100K
UPC_XA_GPIO4 — R3002 100K
UPC_XB_GPIO1 — R3005 100K
UPC_XB_GPIO4 — R3007 100K
UPC_XB_GPIO9 — R3012 100K
UPC_XB_GPIO10 — R3016 100K
UPC_XA_FAULT_L — R3026 100K — PP3V3_S5
UPC_XB_FAULT_L — R3028 100K — PP3V3_S5

RIDGE 0.9V SVR XW

P0V9_TBT_X_SVR_AGND — XW3000 (SM)

POWER ALIASES

(NO_XNET_CONNECTION=1)

PP3V3_UPC_XB_LDO — PP3V3_UPC_XB_LDO (MAKE_BASE=TRUE)
PPVBUS_USBC_XA — PPVBUS_USBC_XA (MAKE_BASE=TRUE, VOLTAGE=20V, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200)
PPVBUS_USBC_XB — PPVBUS_USBC_XB (MAKE_BASE=TRUE, VOLTAGE=20V, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200)
PPVBUS_USBC_XA — PPVBUS_USBC_XA (MAKE_BASE=TRUE)
PPDCIN_XA_G3H_F — PPDCIN_XA_G3H_F (MAKE_BASE=TRUE)
PPVBUS_USBC_XB — PPVBUS_USBC_XB (MAKE_BASE=TRUE)
PPDCIN_XB_G3H_F — PPDCIN_XB_G3H_F (MAKE_BASE=TRUE)
PPDCIN_G3H — PPDCIN_G3H (VOLTAGE=20V, MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200)
PP5V_S4_X_USBC — PP5V_S4_X_USBC (VOLTAGE=5V, MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200)
PP3V3_S0SW_TBT_X_SNS — PP3V3_S0SW_TBT_X_SNS (VOLTAGE=3.3V, MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200)
PP3V3_TBT_X_SX — PP3V3_TBT_X_SX (MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200)

GND ALIASES

GND (MAKE_BASE=TRUE)

PP1V8_AWAKE — R3006 0 1/20W MF 0201 — SOC_USB_VBUS

I2C SERIES R'S

I2C_UPC_X_SDA2 — R3021 33 (PLACE_NEAR=U3900.J4:5mm) — I2C_UPC_SDA
I2C_UPC_X_SCL2 — R3025 33 (PLACE_NEAR=U3900.M3:10mm) — I2C_UPC_SCL

SIGNAL ALIASES

UPC_X_5V_EN — UPC_X_5V_EN (MAKE_BASE=TRUE)
UPC_PMU_RESET — UPC_PMU_RESET (MAKE_BASE=TRUE)
TBT_POC_RESET — TBT_POC_RESET (MAKE_BASE=TRUE)
TBT_X_HDMI_DDC_DATA — TBT_X_HDMI_DDC_DATA (MAKE_BASE=TRUE)
TBT_X_HDMI_DDC_CLK — TBT_X_HDMI_DDC_CLK (MAKE_BASE=TRUE)
SOC_DFU_STATUS — SOC_DFU_STATUS (MAKE_BASE=TRUE)
SOC_FORCE_DFU — SOC_FORCE_DFU (MAKE_BASE=TRUE)

Mobile Config

PP3V3_UPC_XB_LDO — PP3V3_UPC_XB_LDO (MAKE_BASE=TRUE)
PP3V3_UPC_XA_LDO — PP3V3_UPC_XA_LDO (MAKE_BASE=TRUE)

CC Aliases for X side

USBC_XB_CC1 — USBC_XB_CC1 (MAKE_BASE=TRUE)
USBC_XB_CC2 — USBC_XB_CC2 (MAKE_BASE=TRUE)
USBC_XA_CC1 — USBC_XA_CC1 (MAKE_BASE=TRUE)
USBC_XA_CC2 — USBC_XA_CC2 (MAKE_BASE=TRUE)

NC for X side

NC_UPC_XA_VDDIO_CFG — NC_UPC_XA_VDDIO_CFG (MAKE_BASE=TRUE)
NC_UPC_XB_VDDIO_CFG — NC_UPC_XB_VDDIO_CFG (MAKE_BASE=TRUE)

TBT SPI ROM

Portable: rear connector->TBT ROM, front connector->GND
Desktop: XA_SPI -> TBT ROM, XB_SPI -> GND

FLASH ROM:
TBT_X_SPI_CLK
TBT_X_SPI_CS_L
TBT_X_SPI_MOSI
TBT_X_SPI_MISO

Ace:
R3011 15 — UPC_XB_SPI_CLK (IN)
R3013 15 — UPC_XB_SPI_CS_L (IN)
R3015 15 — UPC_XB_SPI_MOSI (IN)
R3019 15 — UPC_XB_SPI_MISO (OUT)

Titan Ridge:
R3022 15 — UPC_X_SPI_CLK (IN)
R3023 15 — UPC_X_SPI_CS_L (IN)
R3024 15 — UPC_X_SPI_MOSI (IN)
R3027 15 — UPC_X_SPI_MISO (OUT)

ACE ARKANOID:
R3029 100 — TBT_X_SPI_ARK_CLK (USBC_DBG)

AARDVARKANOID:
R3030 15 — TBT_X_SPI_DBG_CLK (USBC_DBG) (IN)
R3031 15 — TBT_X_SPI_DBG_CS_L (USBC_DBG) (IN)
R3032 15 — TBT_X_SPI_DBG_MOSI (USBC_DBG) (IN)
R3033 15 — TBT_X_SPI_DBG_MISO (USBC_DBG) (OUT)

SIGNAL ALIASES

USBC_X_RESET_L — USBC_X_RESET_L (MAKE_BASE=TRUE)
TP_USBC_XA_RESET_L — TP_USBC_XA_RESET_L (MAKE_BASE=TRUE)

TBT to ACE

TBT — Titan Ridge U2800 (MASTER)
I2C_TBT_X_SCL
I2C_TBT_X_SDA
I2C_TBT_XA_INT_L
I2C_TBT_XB_INT_L

Pri ACE — U3100 (Write: 0x70 Read: 0x71)
I2C_TBT_X_SCL
I2C_TBT_X_SDA
I2C_TBT_XA_INT_L

Sec ACE — U3200 (Write: 0x7E Read: 0x7F)
I2C_TBT_X_SCL
I2C_TBT_X_SDA
I2C_TBT_XB_INT_L

BOM_COST_GROUP=TBT

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Apple Inc.	DRAWING NUMBER 051-04492 SIZE D
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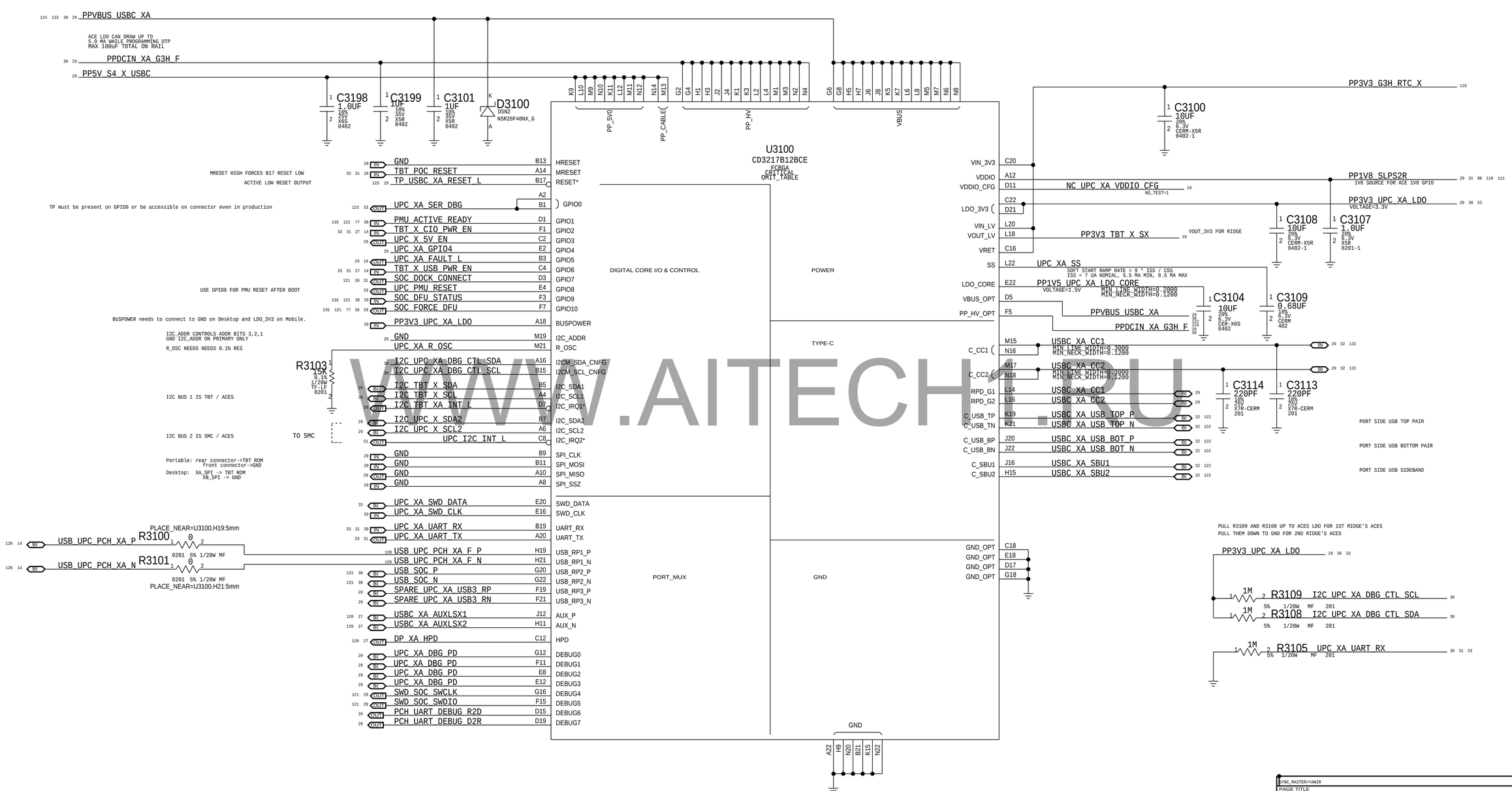
X PRIMARY ACE USB-C PORT CONTROLLER (UPC)



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BOM_COST_GROUP=USB-C

SYNC_MASTER=YANIR SYNC_DATE=01/17/2019

PAGE TITLE: USB-C PORT CONTROLLER XA

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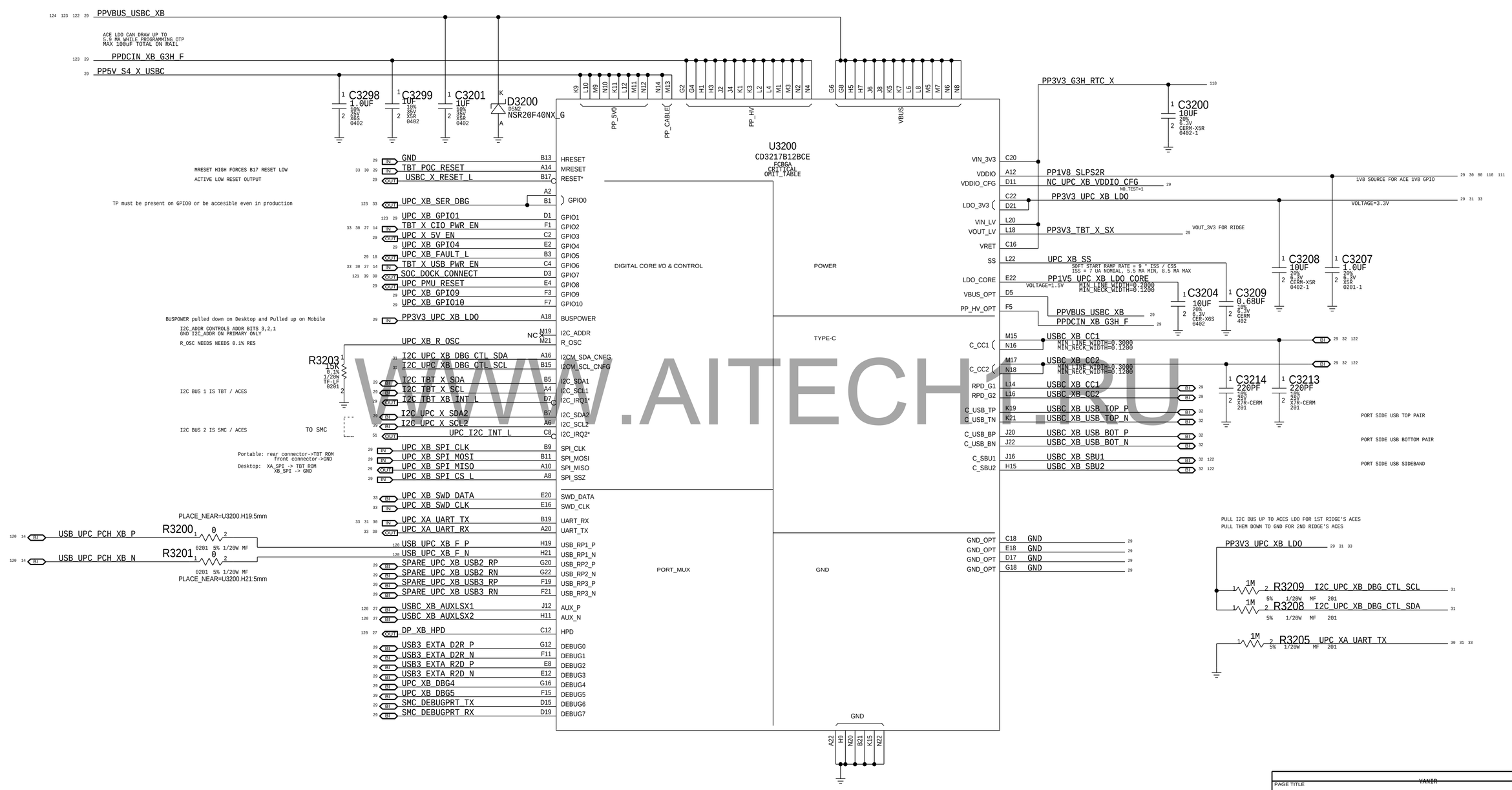
X SECONDARY ACE USB-C PORT CONTROLLER (UPC)



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BOM_COST_GROUP=USB-C

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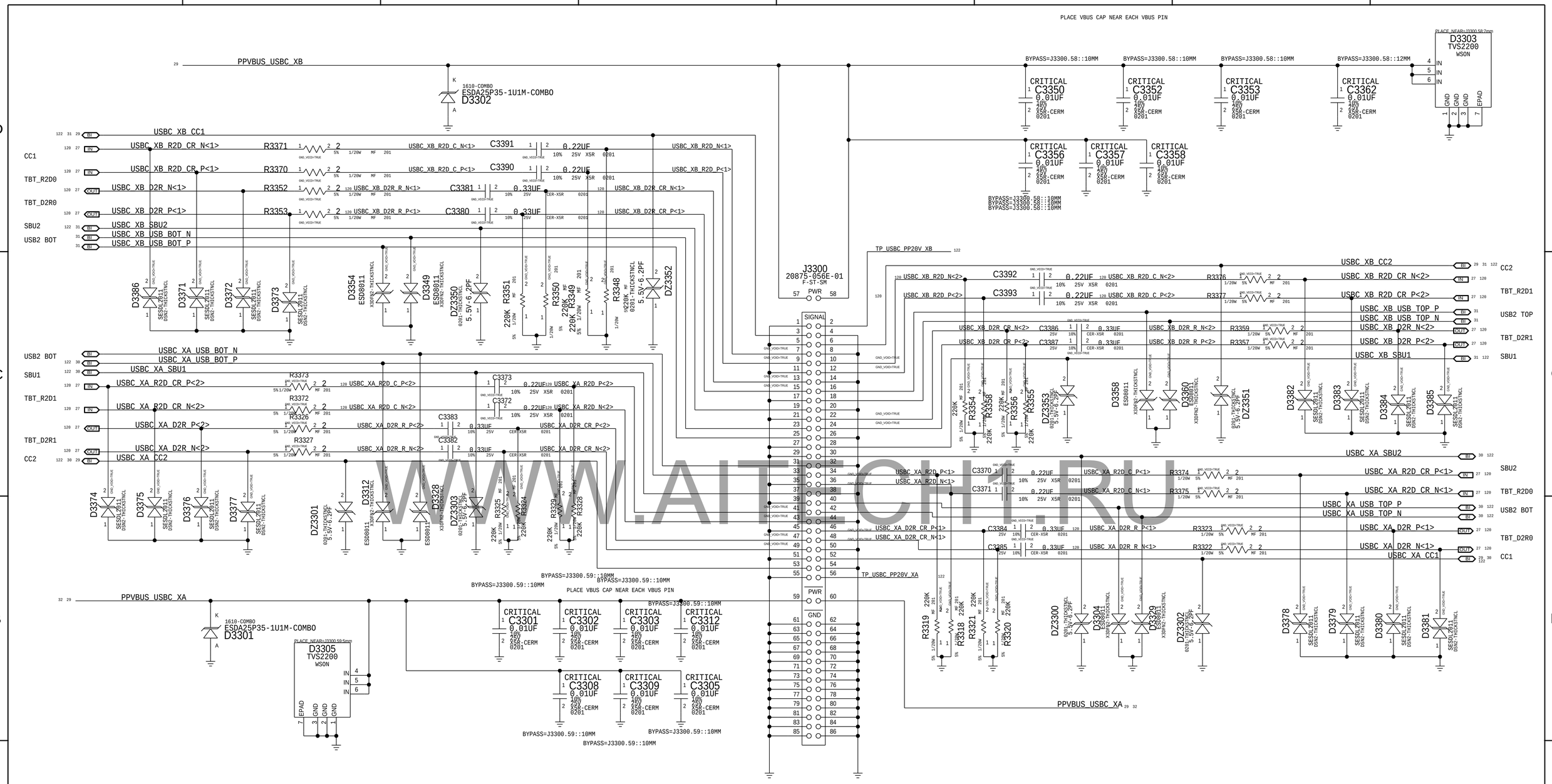

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LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE: USB-C X Connector

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AARDVARKANOID CONN

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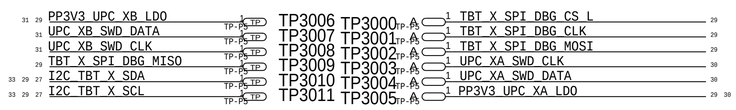

ACE ARKANOID CONN

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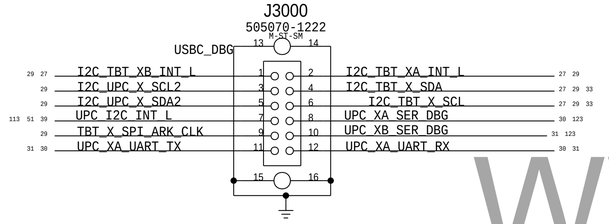
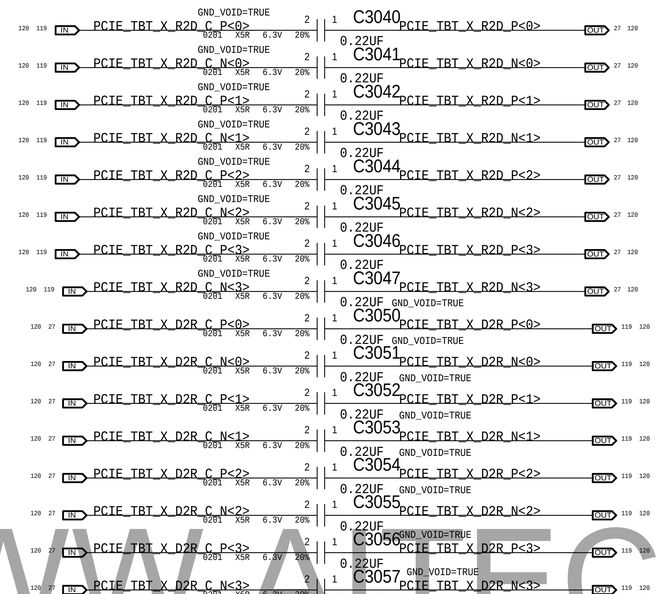


Ridge PCIE Caps



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RIDGE ARKANOID CONN

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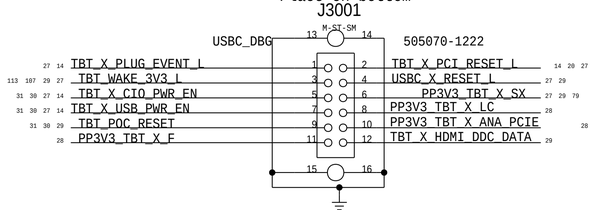

BOM_COST_GROUP=USB-C

DESIGN: X1032/MLB_P4BP
LAST CHANGE: Fri Jan 6 16:01:21 2017

PAGE TITLE
USBC X Connector Support

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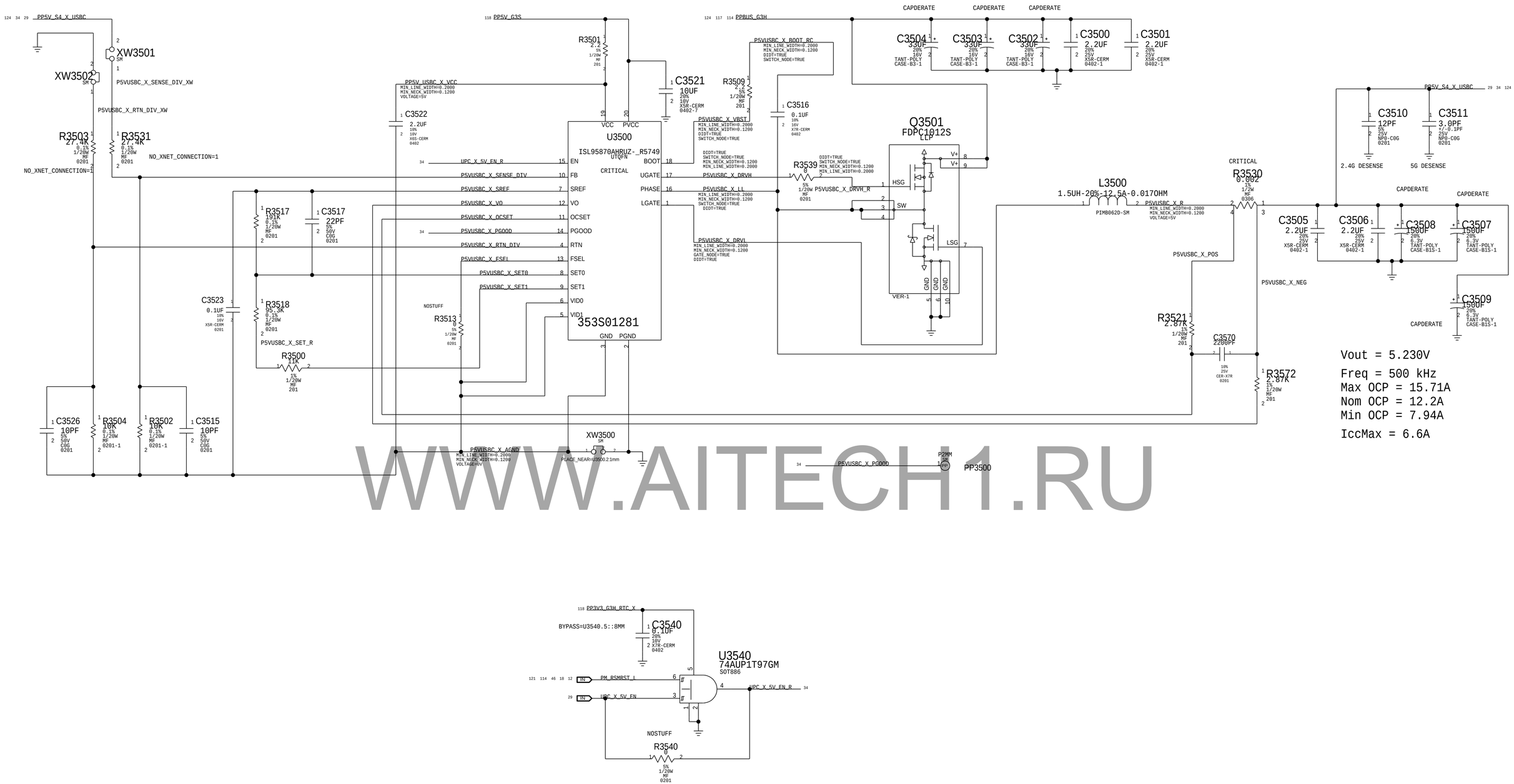

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BOM_COST_GROUP=USB-C

PAGE TITLE
TBT 5V REGULATOR

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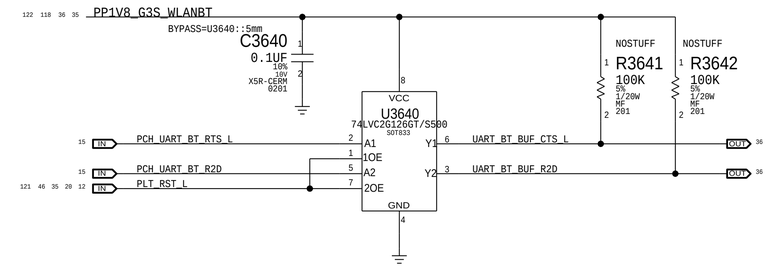
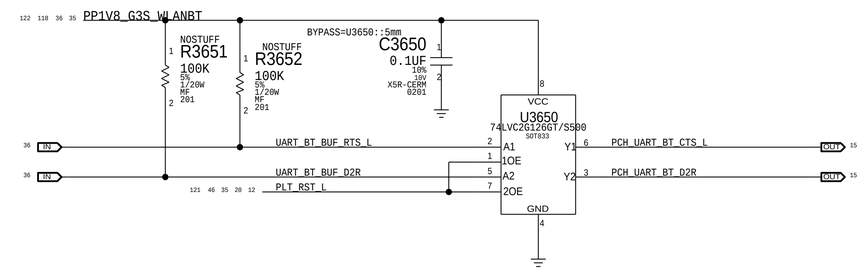


BT UART BUFFERS



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BOM_COST_GROUP=WIRELESS

SYNC_MASTER=METE SYNC_DATE=01/17/2019

PAGE TITLE
WIFI/BT: Support

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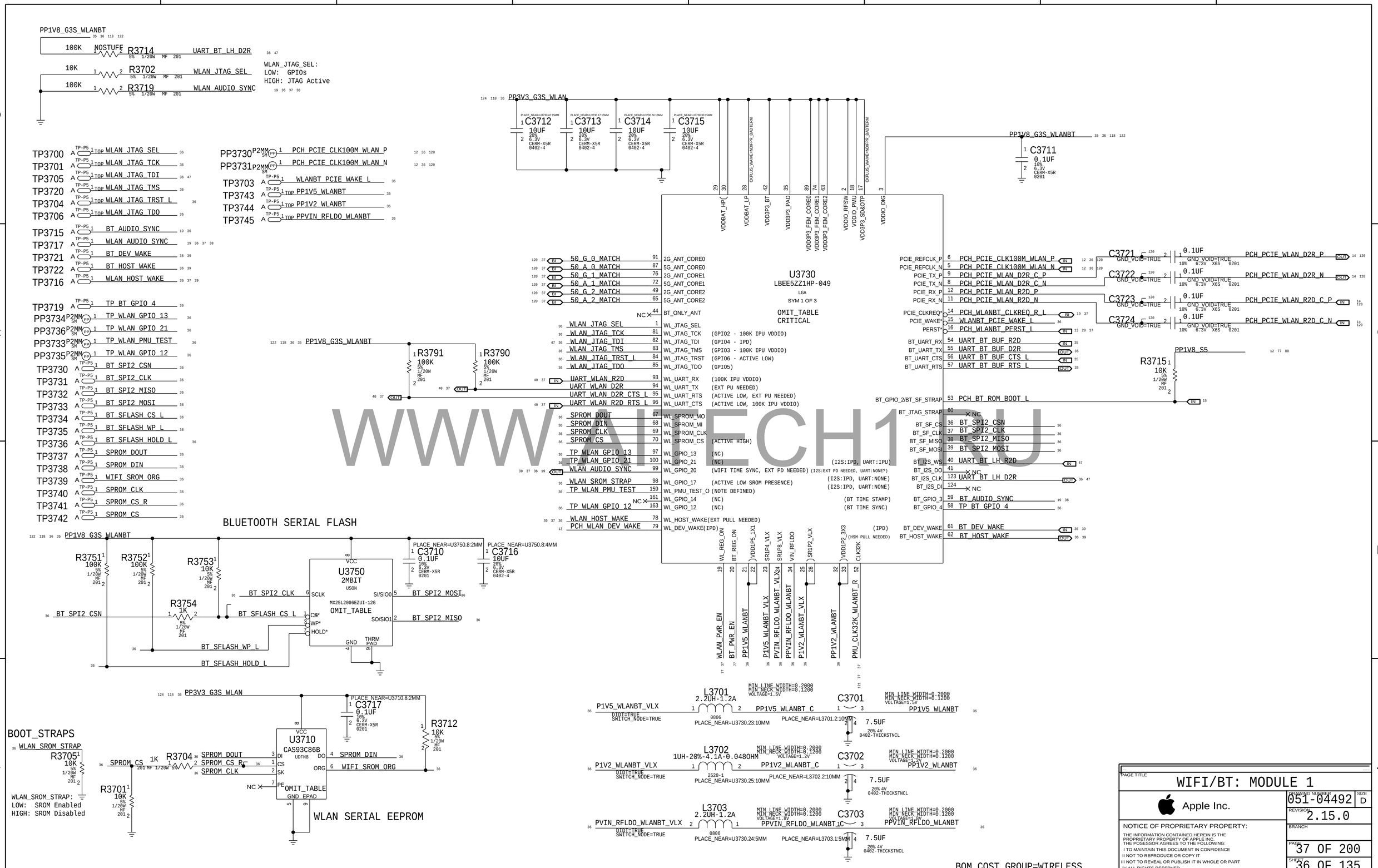
PP1V8_G3S_WLANBT
R3714 100K NOSTUFF UART_BT_LH_D2R
R3702 10K WLAN_JTAG_SEL
R3719 100K WLAN_AUDIO_SYNC
WLAN_JTAG_SEL:
LOW: GPIOs
HIGH: JTAG Active
PP3V3_G3S_WLAN
C3712 10UF
C3713 10UF
C3714 10UF
C3715 10UF
C3711 0.1UF
TP3700 WLAN_JTAG_SEL
TP3701 WLAN_JTAG_TCK
TP3705 WLAN_JTAG_TDI
TP3720 WLAN_JTAG_TMS
TP3704 WLAN_JTAG_TRST_L
TP3706 WLAN_JTAG_TDO
TP3715 BT_AUDIO_SYNC
TP3717 WLAN_AUDIO_SYNC
TP3721 BT_DEV_WAKE
TP3722 BT_HOST_WAKE
TP3716 WLAN_HOST_WAKE
TP3719 TP_BT_GPIO_4
PP3734 TP_WLAN_GPIO_13
PP3736 TP_WLAN_GPIO_21
PP3733 TP_WLAN_PMU_TEST
PP3735 TP_WLAN_GPIO_12
TP3730 BT_SPI2_CSN
TP3731 BT_SPI2_CLK
TP3732 BT_SPI2_MISO
TP3733 BT_SPI2_MOSI
TP3734 BT_SFLASH_CS_L
TP3735 BT_SFLASH_WP_L
TP3736 BT_SFLASH_HOLD_L
TP3737 SPROM_DOUT
TP3738 SPROM_DIN
TP3739 WIFI_SROM_ORG
TP3740 SPROM_CLK
TP3741 SPROM_CS_R
TP3742 SPROM_CS
PP3730 PCH_PCIE_CLK100M_WLAN_P
PP3731 PCH_PCIE_CLK100M_WLAN_N
TP3703 WLANBT_PCIE_WAKE_L
TP3743 PP1V5_WLANBT
TP3744 PP1V2_WLANBT
TP3745 PPVIN_RFLDO_WLANBT
U3730
LBEE5ZZ1HP-049
LGA
SYM 1 OF 3
OMIT_TABLE
CRITICAL
50_G_0_MATCH
50_A_0_MATCH
50_G_1_MATCH
50_A_1_MATCH
50_G_2_MATCH
50_A_2_MATCH
2G_ANT_CORE0
5G_ANT_CORE0
2G_ANT_CORE1
5G_ANT_CORE1
2G_ANT_CORE2
5G_ANT_CORE2
BT_ONLY_ANT
WL_JTAG_SEL
WL_JTAG_TCK (GPIO2 - 100K IPU VDDIO)
WL_JTAG_TDI (GPIO4 - IPD)
WL_JTAG_TMS (GPIO3 - 100K IPU VDDIO)
WL_JTAG_TRST (GPIO6 - ACTIVE LOW)
WL_JTAG_TDO (GPIO5)
WL_UART_RX (100K IPU VDDIO)
WL_UART_TX (EXT PU NEEDED)
WL_UART_RTS (ACTIVE LOW, EXT PU NEEDED)
WL_UART_CTS (ACTIVE LOW, 100K IPU VDDIO)
WL_SPROM_MO
WL_SPROM_MI
WL_SPROM_CLK
WL_SPROM_CS (ACTIVE HIGH)
WL_GPIO_13 (NC)
WL_GPIO_21 (NC)
WL_GPIO_20 (WIFI TIME SYNC, EXT PD NEEDED)
WL_GPIO_17 (ACTIVE LOW SROM PRESENCE)
WL_PMU_TEST_O (NOTE DEFINED)
WL_GPIO_14 (NC)
WL_GPIO_12 (NC)
WL_HOST_WAKE(EXT PULL NEEDED)
WL_DEV_WAKE(IPD)
PCIE_REFCLK_P PCH_PCIE_CLK100M_WLAN_P
PCIE_REFCLK_N PCH_PCIE_CLK100M_WLAN_N
PCIE_TX_P PCH_PCIE_WLAN_D2R_C_P
PCIE_TX_N PCH_PCIE_WLAN_D2R_C_N
PCIE_RX_P PCH_PCIE_WLAN_R2D_P
PCIE_RX_N PCH_PCIE_WLAN_R2D_N
PCIE_CLKREQ* PCH_WLANBT_CLKREQ_R_L
PCIE_WAKE* WLANBT_PCIE_WAKE_L
PERST* PCH_WLANBT_PERST_L
BT_UART_RX UART_BT_BUF_R2D
BT_UART_TX UART_BT_BUF_D2R
BT_UART_CTS UART_BT_BUF_CTS_L
BT_UART_RTS UART_BT_BUF_RTS_L
BT_GPIO_2/BT_SF_STRAP PCH_BT_ROM_BOOT_L
BT_JTAG_STRAP NC
BT_SF_CS BT_SPI2_CSN
BT_SF_CLK BT_SPI2_CLK
BT_SF_MISO BT_SPI2_MISO
BT_SF_MOSI BT_SPI2_MOSI
BT_I2S_WS UART_BT_LH_R2D
BT_I2S_DO NC
BT_I2S_CLK UART_BT_LH_D2R
BT_I2S_DI NC
BT_GPIO_3 BT_AUDIO_SYNC
BT_GPIO_4 TP_BT_GPIO_4
BT_DEV_WAKE
BT_HOST_WAKE
C3721 0.1UF PCH_PCIE_WLAN_D2R_P
C3722 0.1UF PCH_PCIE_WLAN_D2R_N
C3723 0.1UF PCH_PCIE_WLAN_R2D_C_P
C3724 0.1UF PCH_PCIE_WLAN_R2D_C_N
PP1V8_S5
R3715 10K
R3791 100K
R3790 100K
WLAN_JTAG_SEL
WLAN_JTAG_TCK
WLAN_JTAG_TDI
WLAN_JTAG_TMS
WLAN_JTAG_TRST_L
WLAN_JTAG_TDO
UART_WLAN_R2D
UART_WLAN_D2R
UART_WLAN_D2R_CTS_L
UART_WLAN_R2D_RTS_L
SPROM_DOUT
SPROM_DIN
SPROM_CLK
SPROM_CS
TP_WLAN_GPIO_13
TP_WLAN_GPIO_21
WLAN_AUDIO_SYNC
WLAN_SROM_STRAP
TP_WLAN_PMU_TEST
TP_WLAN_GPIO_12
WLAN_HOST_WAKE
PCH_WLAN_DEV_WAKE
BLUETOOTH SERIAL FLASH
PP1V8_G3S_WLANBT
R3751 100K
R3752 100K
R3753 10K
R3754 1K
U3750
2MBIT
USON
MX25L2006EZUI-12G
OMIT_TABLE
BT_SPI2_CLK
BT_SPI2_CSN
BT_SFLASH_CS_L
BT_SFLASH_WP_L
BT_SFLASH_HOLD_L
BT_SPI2_MOSI
BT_SPI2_MISO
C3710 0.1UF
C3716 10UF
PP3V3_G3S_WLAN
C3717 0.1UF
BOOT_STRAPS
WLAN_SROM_STRAP
R3705 10K
R3704 1K
R3701 10K
R3712 10K
U3710
CAS93C86B
UDFN8
OMIT_TABLE
SPROM_DOUT
SPROM_CS_R
SPROM_CLK
SPROM_CS
SPROM_DIN
WIFI_SROM_ORG
WLAN_SROM_STRAP:
LOW: SROM Enabled
HIGH: SROM Disabled
WLAN SERIAL EEPROM
WL_REG_ON
BT_REG_ON
VDD1P5_1X1
SR1P4_VLX
SR1P8_VLX
VIN_RFLDO
SR1P2_VLX
VDD1P2_3X3
CLK32K
WLAN_PWR_EN
BT_PWR_EN
PP1V5_WLANBT
P1V5_WLANBT_VLX
PVIN_RFLDO_WLANBT_VLX
PPVIN_RFLDO_WLANBT
P1V2_WLANBT_VLX
PP1V2_WLANBT
PMU_CLK32K_WLANBT_R
L3701 2.2UH-1.2A
C3701 7.5UF
PP1V5_WLANBT_C
L3702 1UH-20%-4.1A-0.0480HM
C3702 7.5UF
PP1V2_WLANBT_C
L3703 2.2UH-1.2A
C3703 7.5UF
PPVIN_RFLDO_WLANBT_C
BOM_COST_GROUP=WIRELESS
PAGE TITLE
WIFI/BT: MODULE 1
Apple Inc.
DRAWING NUMBER 051-04492
SIZE D
REVISION 2.15.0
BRANCH
PAGE 37 OF 200
SHEET 36 OF 135
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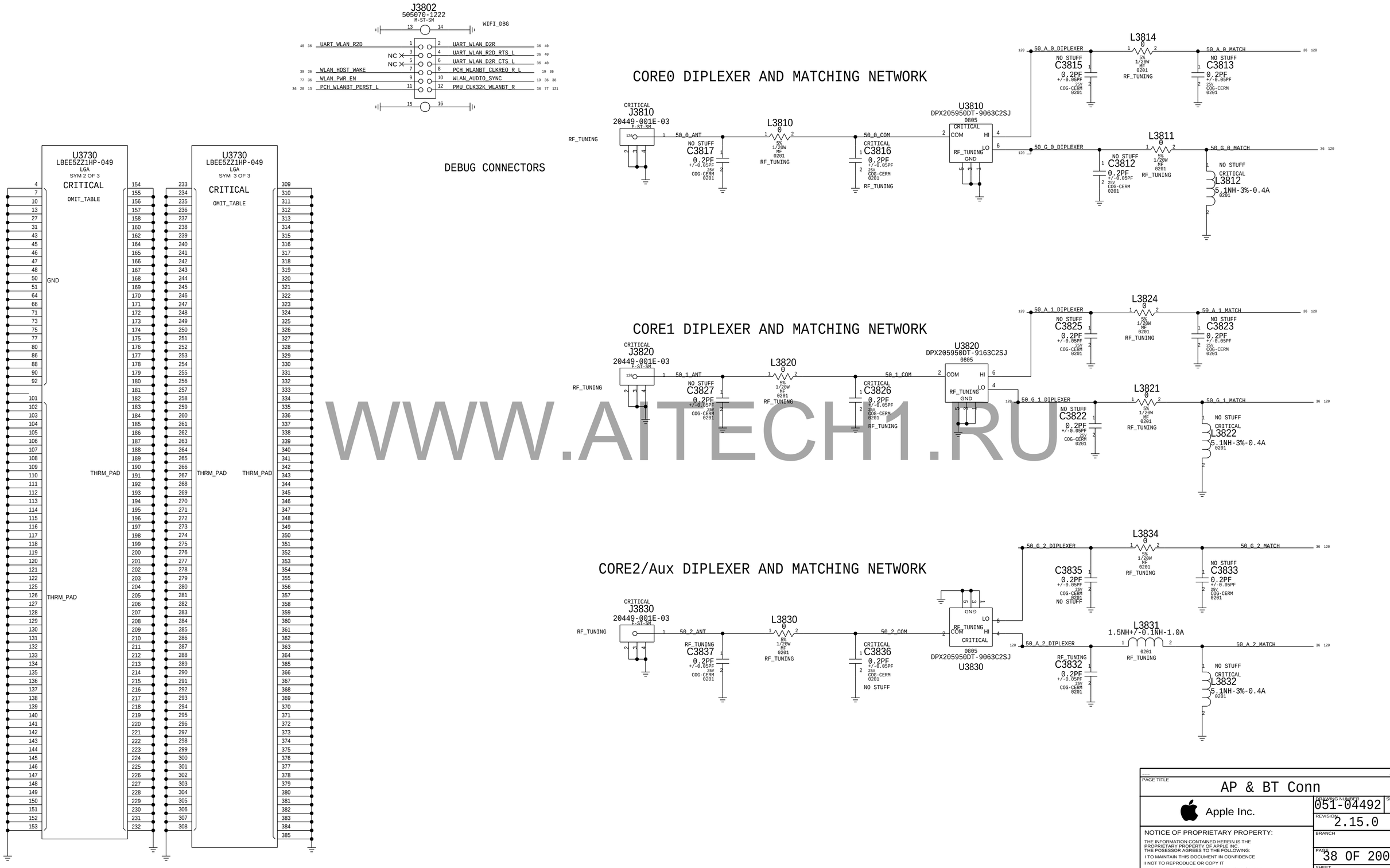

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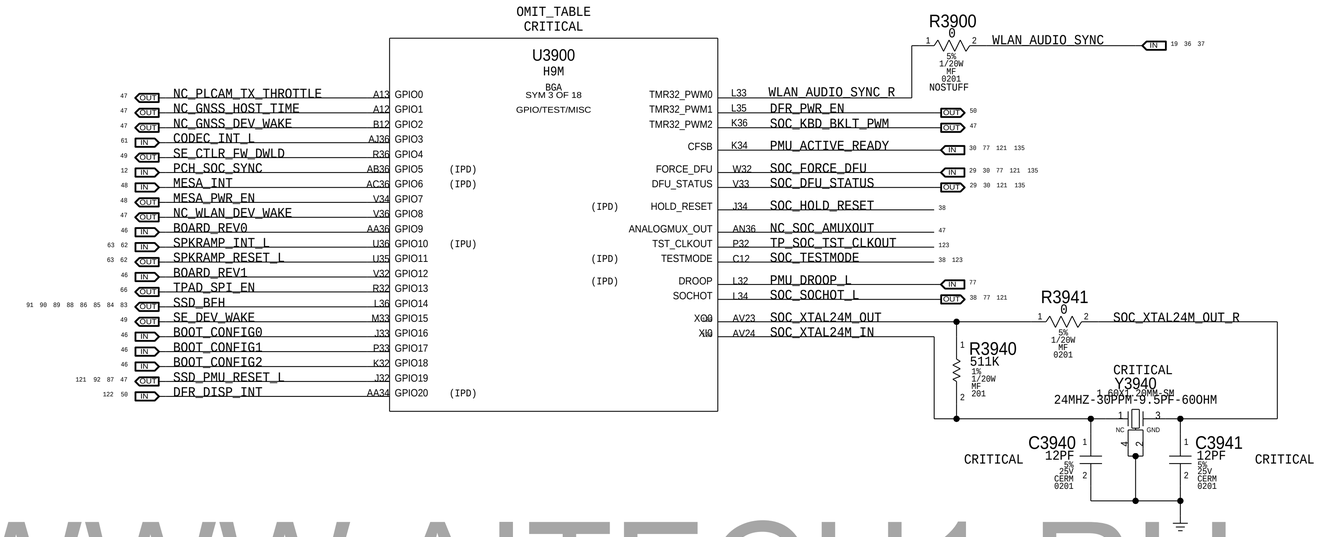
Note 1) IPU represents SW configured state, not HW default



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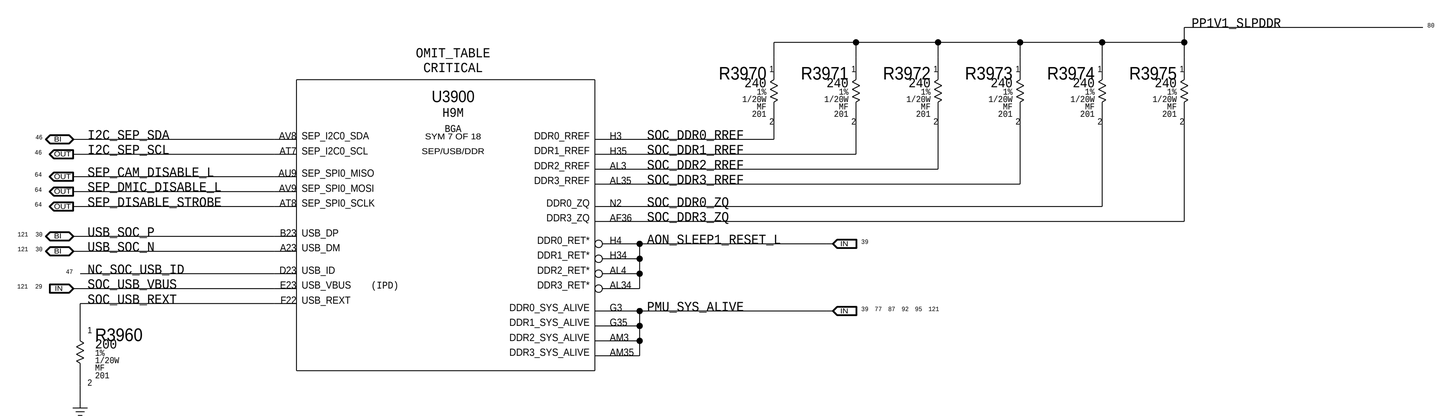

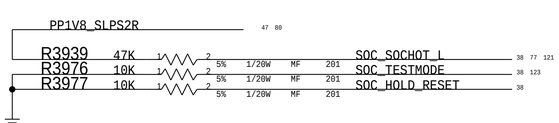

BOM_COST_GROUP=SOC

SYNC_MASTER=ANDY SYNC_DATE=01/17/2010

PAGE TITLE
SoC GPIO/SEP/USB/DDR/Test

Apple Inc.

DRAWING NUMBER 051-04492
SIZE D
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OMIT_TABLE
CRITICAL

U3900
H9M
BGA
SYM 6 OF 18
AOP

47	OUT	NC_WLAN_CONTEXT_A	D3	AOP_FUNC[0]		AOP_PDM_CLK0	P6	PDM_DMIC_CLK0_R
47	OUT	NC_WLAN_CONTEXT_B	F4	AOP_FUNC[1]		AOP_PDM_CLK1	K2	PDM_DMIC_CLK1_R
47	IN	NC_GYRO_INT1	M6	AOP_FUNC[2]	(IPD)	AOP_PDM_CLK2 (IPU)	J6	SMC_FIXTURE_MODE_L
47	IN	NC_GYRO_INT2	D4	AOP_FUNC[3]	(IPD)	AOP_PDM_CLK3 (IPU)	L6	NC_PLCAM_PROX_INT_L
47	IN	SE_HOST_WAKE_R	F3	AOP_FUNC[4]		AOP_PDM_CLK4 (IPU)	L5	NC_PLCAM_ROMEO_B2B_DETECT
20 15	IN	SOC_PERST_L	K6	AOP_FUNC[5]				
47	IN	NC_ALTIMETER_INT	E4	AOP_FUNC[6]	(IPD)	AOP_PDM_DATA0 (IPD)	J5	PDM_DMIC_DATA0
47	OUT	NC_SPI_GYRO_CS_L	J3	AOP_FUNC[7]		AOP_PDM_DATA1 (IPD)	K4	PDM_DMIC_DATA1
47	OUT	SPI_AOP_MA781_CS_L	H6	AOP_FUNC[8]				
						AOP_SPI_MOSI	D2	SPI_AOP_SENSOR_MOSI_R
47	OUT	NC_I2C_AOP_SCL	N6	AOP_I2C0_SCL		AOP_SPI_SCLK	F2	SPI_AOP_SENSOR_CLK_R
47	BI	NC_I2C_AOP_SDA	G5	AOP_I2C0_SDA		AOP_SPI_MISO	E2	SPI_AOP_SENSOR_MISO

OMIT_TABLE
CRITICAL

U3900
H9M
BGA
SYM 5 OF 18
AON

122 50	IN	DFR_TOUCH_INT_L	AL6	AON_GPIO0		JTAG_TCK (IPU)	AK6	SWD_SOC_SWCLK
46	IN	CPU_SMC_THRMTRIP_L	AE6	AON_GPIO1	(IPU)	JTAG_TMS (IPU)	AN5	SWD_SOC_SWDIO
119 97	IN	GFX_SELF_THROTTLE_1V8	AT5	AON_GPIO2	(IPD)	JTAG_TDI (IPU)	AH6	TP_JTAG_SOC_TDI
47	OUT	SMC_GPU_THRMTRIP	AN4	AON_GPIO3		JTAG_TDO	AP4	TP_JTAG_SOC_TDO
18	IN	XDP_PRESENT_L	AK4	AON_GPIO4		JTAG_TRST* (IPD)	AJ6	TP_JTAG_SOC_TRST_L
61	OUT	CODEC_RESET_L	AV5	AON_GPIO5		JTAG_SEL	AC6	SOC_JTAG_SEL (DAP=0, TAP=1)
36	OUT	BT_DEV_WAKE	AR3	AON_GPIO6				
47	IN	NC_PCIEDN_WAKE_L	AG6	AON_GPIO7	(IPU)	DOCK_CONNECT	AN2	SOC_DOCK_CONNECT
47	OUT	NC_ENET_LOW_PWR	AU5	AON_GPIO8				
47	IN	TPAD_SPI_INT_L	AP2	AON_GPIO9		AON_SWD0_TMS	AJ4	NC_SWD_WLAN_SWDIO
47	IN	NC_SDCONN_STATE_CHANGE_L	AR4	AON_GPIO10	(IPU)	AON_SWD1_TMS (IPU)	AH4	NC_MESA_MENUKEY_L
47	IN	NC_ENET_MEDIA_SENSE	AN3	AON_GPIO11	(IPD)	AON_SWD01_TCK	AJ2	NC_SWD_WLAN_SWCLK
77	IN	PMU_INT_L	AT6	AON_GPIO12	(IPU)			
						WDOG	AJ5	SOC_WDOG
						AON_SLEEP1_RESET*	AF6	AON_SLEEP1_RESET_L

CKPLUS_WAIVE=SINGLE_COMP_NET

77	OUT	SPMI_CLK	R4036	20	5% 1/20W MF 201	SPMI_CLK_R	AD6	AON_SPMI_SCLK
77	BI	SPMI_DATA	R4037	20	5% 1/20W MF 201	SPMI_DATA_R	AR2	AON_SPMI_SDATA
123 121 77	IN	PMU_CLK32K_SOC					AR5	RT_CLK32768
		SOC_COLD_RESET_L					AK2	COLD_RESET*
			R4039	4.7K	5% 1/20W MF 201		AK3	CFSB_AON
121 77 64	IN	PMU_COLD_RESET_L						

PLACE_NEAR=U3900.AD6:5MM
PLACE_NEAR=U7800.M7:5MM

OMIT_TABLE
CRITICAL

U3900
H9M
BGA
SYM 9 OF 18
SMC

120 39 12	BI	ESPI_IO<0>	V2	SMC_ESPI_IO0		SMC_GPIO0	Y4	CODEC_WAKE_L
120 39 12	BI	ESPI_IO<1>	U3	SMC_ESPI_IO1		SMC_GPIO1 (IPD)	Y8	BT_HOST_WAKE
120 39 12	BI	ESPI_IO<2>	U4	SMC_ESPI_IO2		SMC_GPIO2 (IPD)	Y5	WLAN_HOST_WAKE
120 39 12	BI	ESPI_IO<3>	V8	SMC_ESPI_IO3		SMC_GPIO3	AA2	GFX_THROTTLE_1V8_L
120 12	IN	ESPI_CLK60M_PCH	U2	SMC_ESPI_CLK	(IPD)	SMC_GPIO4	Y7	LID_OPEN_SMC_IN
120 39 12	IN	ESPI_CS_L	V3	SMC_ESPI_CS*		SMC_GPIO5 (IPD)	Y6	PCC_EVENT
121 120 12	IN	ESPI_RESET_L	V6	SMC_ESPI_RESET*	(IPD)	SMC_GPIO6	AB2	NC_TPAD_VIBE_L
						SMC_GPIO7	AD5	TPAD_KBD_WAKE_L
46	IN	SMC_PECI_RX	M5	SMC_PECI_IN	(IPD)	SMC_GPIO8	AD2	NC_LIDOPEN_PSU12VPGOOD_ACDCBURST_L
46	OUT	SMC_PECI_TX	T6	SMC_PECI_OUT		SMC_GPIO9	AB4	NC_SPI_DESCRIPTOR_OVERRIDE_L
123 46	OUT	SMC_PCH_PWROK	W7	PCH_PWROK		SMC_GPIO10 (IPU)	AC2	DISP_GCON_INT_L
123 46	OUT	SMC_PCH_SYS_PWROK	W8	SYS_PWROK		SMC_GPIO11	AC3	PCH_GCON_INT_L
						SMC_GPIO12	AA8	NC_TPAD_ACTUATOR_DISABLE_L
46	OUT	SMC_RSMRST_L	W6	RSMRST*		SMC_GPIO13 (IPU)	AB3	TBT_WAKE_L
121 46	OUT	SMC_SYSRST_L	W4	SYS_RESET*		SMC_GPIO14 (IPU)	AE2	UPC_I2C_INT_L
135 121 77 12	IN	PM_SLP_S0_L	AA4	SLP_S0B		SMC_GPIO15 (IPD)	L4	NC_GNSS_HOST_WAKE
69 47 46	BI	SMC_PROCHOT_L	R5	PROCHOT*				
						SMC_ADC0	AG2	SMC_DCIN_VSENSE
						SMC_ADC1	AC4	SMC_DCIN_ISENSE
						SMC_ADC2	AH3	SMC_PBUS_VSENSE
						SMC_ADC3	AD4	SMC_BMON_ISENSE
						SMC_ADC4	AB6	SMC_CPU_HI_ISENSE
						SMC_ADC5	AH2	SMC_GPU_HS_ISENSE
						SMC_ADC6	AG4	SMC_P3V3_WLAN_ISENSE
						SMC_ADC7	AC5	SMC_P3V3_CAPLE_ISENSE
121 95 92 87 77 38	IN	PMU_SYS_ALIVE	AA6	SYS_ALIVE				
						REFP_ADC	AF4	PP1V25_SLPS2R_SMC_AVREF
						~~REFM_ADC~~	AG3	GND_SMC_AVSS
121 51	OUT	I2C_UPC_SCL	M3	SMC_I2C0_SCL				
121 51	BI	I2C_UPC_SDA	J4	SMC_I2C0_SDA				
51	OUT	I2C_SNS0_S0_SCL	N4	SMC_I2C1_SCL				
51	BI	I2C_SNS0_S0_SDA	P4	SMC_I2C1_SDA				
51	OUT	I2C_SNS1_S0_SCL	U5	SMC_I2C2_SCL				
51	BI	I2C_SNS1_S0_SDA	M2	SMC_I2C2_SDA				
51	OUT	I2C_DISP_SCL	U6	SMC_I2C3_SCL				
51	BI	I2C_DISP_SDA	R4	SMC_I2C3_SDA				
121 51	OUT	I2C_PWR_SCL	P3	SMC_I2C4_SCL				
121 51	BI	I2C_PWR_SDA	T4	SMC_I2C4_SDA				
51	OUT	I2C_SNS_G3S_SCL	R2	SMC_I2C5_SCL				
51	BI	I2C_SNS_G3S_SDA	P2	SMC_I2C5_SDA				
51	OUT	I2C_SSD_SCL	R3	SMC_I2C6_SCL				
51	BI	I2C_SSD_SDA	T2	SMC_I2C6_SDA				
						SMC_PWM0	J2	SMC_FAN_0_PWM
						SMC_TACH0	L3	SMC_FAN_0_TACH
						SMC_PWM1	R6	SMC_FAN_1_PWM
						SMC_TACH1	L2	SMC_FAN_1_TACH
						SMC_PWM2	M4	NC_SMC_LED_ONEWIRE
						SMC_UART0_RXD (IPU)	V4	SMC_DEBUGPRT_RX
						SMC_UART0_TXD	V5	SMC_DEBUGPRT_TX
						SWD_OUT0_TCK	AE3	SSD0_SWCLK_UART_R2D
						SWD_OUT0_TMS	AA5	SSD0_SWDIO_UART_D2R
						SWD_OUT1_TCK	AF2	SSD1_SWCLK_UART_R2D
						SWD_OUT1_TMS	AA7	SSD1_SWDIO_UART_D2R

47	IN	SMC_DCIN_VSENSE	59
47	IN	SMC_DCIN_ISENSE	59
47	IN	SMC_PBUS_VSENSE	59
47	IN	SMC_BMON_ISENSE	59
47	IN	SMC_CPU_HI_ISENSE	59
47	IN	SMC_GPU_HS_ISENSE	59
47	IN	SMC_P3V3_WLAN_ISENSE	59
47	IN	SMC_P3V3_CAPLE_ISENSE	59
46		PP1V25_SLPS2R_SMC_AVREF	
123 58		GND_SMC_AVSS	
47	OUT	SMC_FAN_0_PWM	59
47	IN	SMC_FAN_0_TACH	59
47	OUT	SMC_FAN_1_PWM	59
47	IN	SMC_FAN_1_TACH	59
47	BI	NC_SMC_LED_ONEWIRE	47
29 121	IN	SMC_DEBUGPRT_RX	29 121
29 121	OUT	SMC_DEBUGPRT_TX	29 121
88 89 90 91 123	OUT	SSD0_SWCLK_UART_R2D	88 89 90 91 123
88 89 90 91 123	BI	SSD0_SWDIO_UART_D2R	88 89 90 91 123
83 84 85 86 123	OUT	SSD1_SWCLK_UART_R2D	83 84 85 86 123
83 84 85 86 123	BI	SSD1_SWDIO_UART_D2R	83 84 85 86 123

XW4089
SM
PLACE_NEAR=U3900.AF3:4MM

PP1V8_S5 — 80

R4046	10K	5% 1/20W MF 201	SOC_JTAG_SEL	39 123
R4047	100K	5% 1/20W MF 201	SOC_DOCK_CONNECT	30 31 39 121
R4054	100K	5% 1/20W MF 201	ESPI_IO<0>	12 39 120
R4055	100K	5% 1/20W MF 201	ESPI_IO<1>	12 39 120
R4056	100K	5% 1/20W MF 201	ESPI_IO<2>	12 39 120
R4057	100K	5% 1/20W MF 201	ESPI_IO<3>	12 39 120
R4059	100K	5% 1/20W MF 201	ESPI_CS_L	12 39 120

BOM_COST_GROUP=SOC

SYNC_MASTER=ANDY — SYNC_DATE=02/19/2019

PAGE TITLE
SoC AOP/AON/SMC

Apple Inc.

DRAWING NUMBER: 051-04492
SIZE: D
REVISION: 2.15.0
BRANCH:
PAGE: 40 OF 200
SHEET: 39 OF 135

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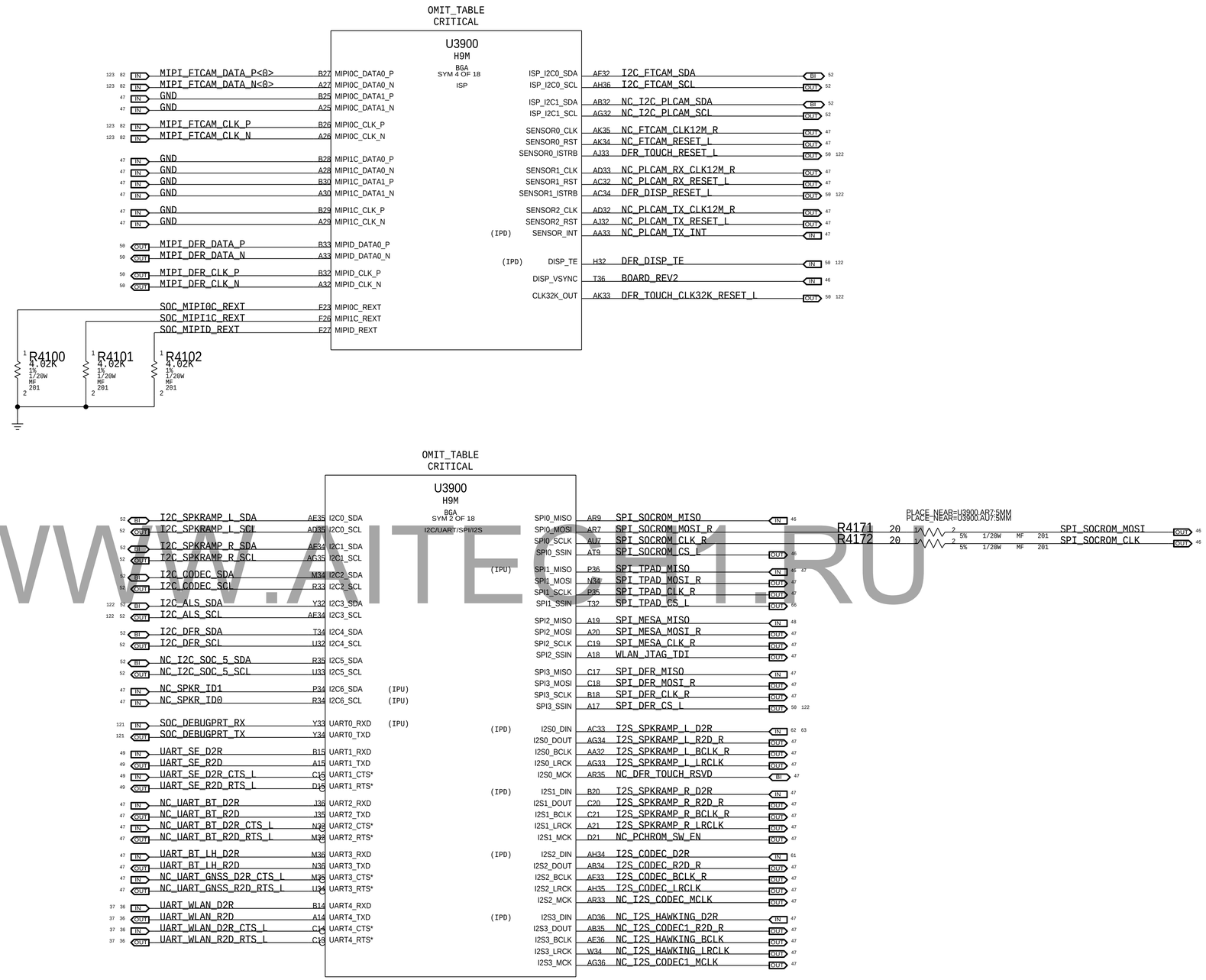

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BOM_COST_GROUP=SOC

SYNC_MASTER= SYNC_DATE=01/17/2019

PAGE TITLE

SoC ISP/I2C/UART/SPI/I2S

Apple Inc.

DRAWING NUMBER 051-04492 SIZE D

REVISION 2.15.0

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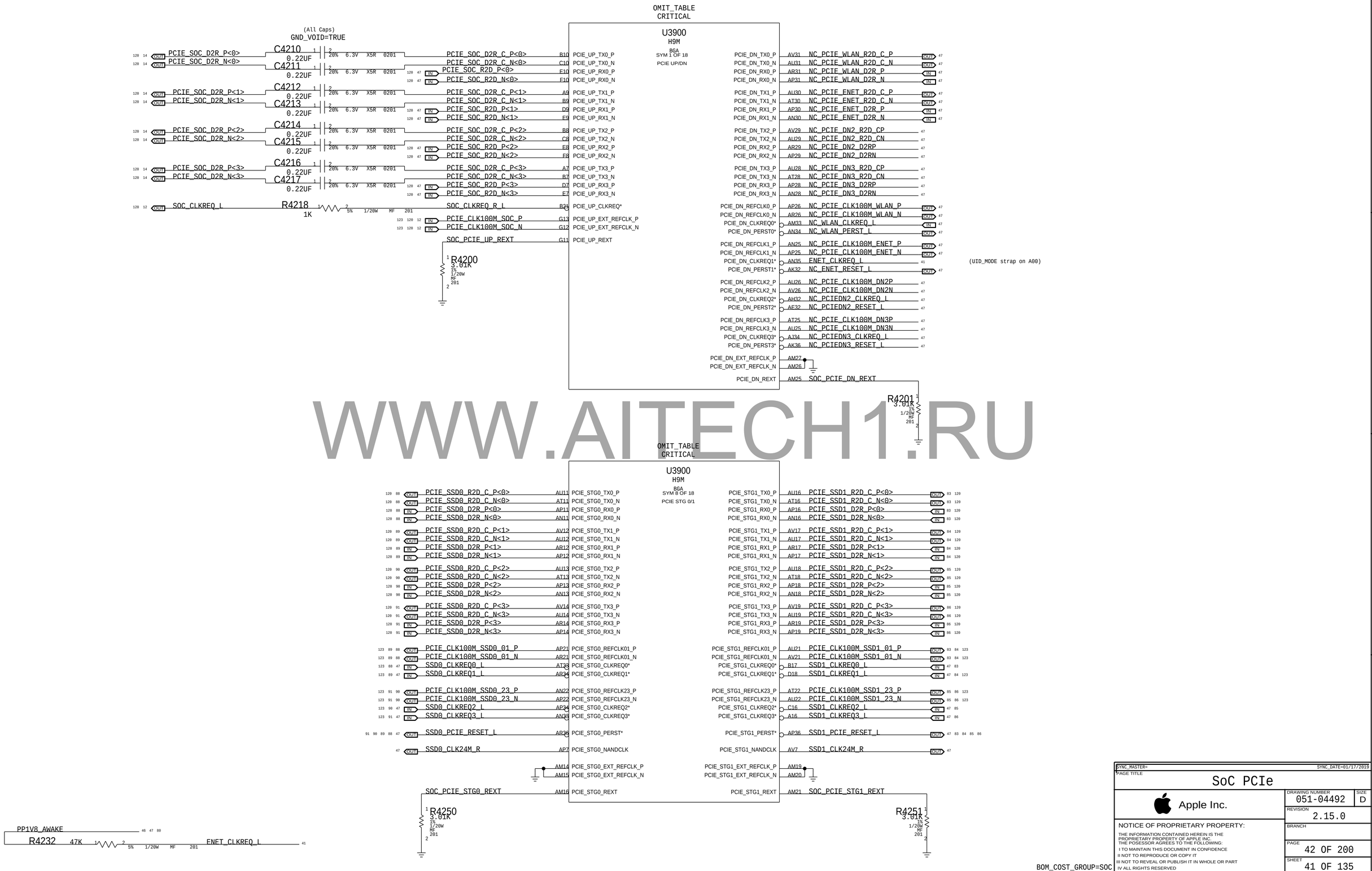
OMIT_TABLE
CRITICAL
U3900
H9M
BGA
SYM 1 OF 18
PCIE UP/DN
(All Caps)
GND_VOID=TRUE
PCIE_SOC_D2R_P<0>
PCIE_SOC_D2R_N<0>
PCIE_SOC_D2R_P<1>
PCIE_SOC_D2R_N<1>
PCIE_SOC_D2R_P<2>
PCIE_SOC_D2R_N<2>
PCIE_SOC_D2R_P<3>
PCIE_SOC_D2R_N<3>
C4210 0.22UF
C4211 0.22UF
C4212 0.22UF
C4213 0.22UF
C4214 0.22UF
C4215 0.22UF
C4216 0.22UF
C4217 0.22UF
SOC_CLKREQ_L
R4218 1K
PCIE_SOC_D2R_C_P<0>
PCIE_SOC_D2R_C_N<0>
PCIE_SOC_R2D_P<0>
PCIE_SOC_R2D_N<0>
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PCIE_SOC_D2R_C_N<1>
PCIE_SOC_R2D_P<1>
PCIE_SOC_R2D_N<1>
PCIE_SOC_D2R_C_P<2>
PCIE_SOC_D2R_C_N<2>
PCIE_SOC_R2D_P<2>
PCIE_SOC_R2D_N<2>
PCIE_SOC_D2R_C_P<3>
PCIE_SOC_D2R_C_N<3>
PCIE_SOC_R2D_P<3>
PCIE_SOC_R2D_N<3>
SOC_CLKREQ_R_L
PCIE_CLK100M_SOC_P
PCIE_CLK100M_SOC_N
SOC_PCIE_UP_REXT
R4200 3.01K
PCIE_UP_TX0_P
PCIE_UP_TX0_N
PCIE_UP_RX0_P
PCIE_UP_RX0_N
PCIE_UP_TX1_P
PCIE_UP_TX1_N
PCIE_UP_RX1_P
PCIE_UP_RX1_N
PCIE_UP_TX2_P
PCIE_UP_TX2_N
PCIE_UP_RX2_P
PCIE_UP_RX2_N
PCIE_UP_TX3_P
PCIE_UP_TX3_N
PCIE_UP_RX3_P
PCIE_UP_RX3_N
PCIE_UP_CLKREQ*
PCIE_UP_EXT_REFCLK_P
PCIE_UP_EXT_REFCLK_N
PCIE_UP_REXT
PCIE_DN_TX0_P
PCIE_DN_TX0_N
PCIE_DN_RX0_P
PCIE_DN_RX0_N
PCIE_DN_TX1_P
PCIE_DN_TX1_N
PCIE_DN_RX1_P
PCIE_DN_RX1_N
PCIE_DN_TX2_P
PCIE_DN_TX2_N
PCIE_DN_RX2_P
PCIE_DN_RX2_N
PCIE_DN_TX3_P
PCIE_DN_TX3_N
PCIE_DN_RX3_P
PCIE_DN_RX3_N
PCIE_DN_REFCLK0_P
PCIE_DN_REFCLK0_N
PCIE_DN_CLKREQ0*
PCIE_DN_PERST0*
PCIE_DN_REFCLK1_P
PCIE_DN_REFCLK1_N
PCIE_DN_CLKREQ1*
PCIE_DN_PERST1*
PCIE_DN_REFCLK2_P
PCIE_DN_REFCLK2_N
PCIE_DN_CLKREQ2*
PCIE_DN_PERST2*
PCIE_DN_REFCLK3_P
PCIE_DN_REFCLK3_N
PCIE_DN_CLKREQ3*
PCIE_DN_PERST3*
PCIE_DN_EXT_REFCLK_P
PCIE_DN_EXT_REFCLK_N
PCIE_DN_REXT
NC_PCIE_WLAN_R2D_C_P
NC_PCIE_WLAN_R2D_C_N
NC_PCIE_WLAN_D2R_P
NC_PCIE_WLAN_D2R_N
NC_PCIE_ENET_R2D_C_P
NC_PCIE_ENET_R2D_C_N
NC_PCIE_ENET_D2R_P
NC_PCIE_ENET_D2R_N
NC_PCIE_DN2_R2D_CP
NC_PCIE_DN2_R2D_CN
NC_PCIE_DN2_D2RP
NC_PCIE_DN2_D2RN
NC_PCIE_DN3_R2D_CP
NC_PCIE_DN3_R2D_CN
NC_PCIE_DN3_D2RP
NC_PCIE_DN3_D2RN
NC_PCIE_CLK100M_WLAN_P
NC_PCIE_CLK100M_WLAN_N
NC_WLAN_CLKREQ_L
NC_WLAN_PERST_L
NC_PCIE_CLK100M_ENET_P
NC_PCIE_CLK100M_ENET_N
ENET_CLKREQ_L
NC_ENET_RESET_L
(UID_MODE strap on A00)
NC_PCIE_CLK100M_DN2P
NC_PCIE_CLK100M_DN2N
NC_PCIEDN2_CLKREQ_L
NC_PCIEDN2_RESET_L
NC_PCIE_CLK100M_DN3P
NC_PCIE_CLK100M_DN3N
NC_PCIEDN3_CLKREQ_L
NC_PCIEDN3_RESET_L
SOC_PCIE_DN_REXT
R4201 3.01K
WWW.AITECH1.RU
OMIT_TABLE
CRITICAL
U3900
H9M
BGA
SYM 8 OF 18
PCIE STG 0/1
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PCIE_SSD0_R2D_C_N<0>
PCIE_SSD0_D2R_P<0>
PCIE_SSD0_D2R_N<0>
PCIE_SSD0_R2D_C_P<1>
PCIE_SSD0_R2D_C_N<1>
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PCIE_SSD0_R2D_C_P<3>
PCIE_SSD0_R2D_C_N<3>
PCIE_SSD0_D2R_P<3>
PCIE_SSD0_D2R_N<3>
PCIE_CLK100M_SSD0_01_P
PCIE_CLK100M_SSD0_01_N
SSD0_CLKREQ0_L
SSD0_CLKREQ1_L
PCIE_CLK100M_SSD0_23_P
PCIE_CLK100M_SSD0_23_N
SSD0_CLKREQ2_L
SSD0_CLKREQ3_L
SSD0_PCIE_RESET_L
SSD0_CLK24M_R
PCIE_STG0_TX0_P
PCIE_STG0_TX0_N
PCIE_STG0_RX0_P
PCIE_STG0_RX0_N
PCIE_STG0_TX1_P
PCIE_STG0_TX1_N
PCIE_STG0_RX1_P
PCIE_STG0_RX1_N
PCIE_STG0_TX2_P
PCIE_STG0_TX2_N
PCIE_STG0_RX2_P
PCIE_STG0_RX2_N
PCIE_STG0_TX3_P
PCIE_STG0_TX3_N
PCIE_STG0_RX3_P
PCIE_STG0_RX3_N
PCIE_STG0_REFCLK01_P
PCIE_STG0_REFCLK01_N
PCIE_STG0_CLKREQ0*
PCIE_STG0_CLKREQ1*
PCIE_STG0_REFCLK23_P
PCIE_STG0_REFCLK23_N
PCIE_STG0_CLKREQ2*
PCIE_STG0_CLKREQ3*
PCIE_STG0_PERST*
PCIE_STG0_NANDCLK
PCIE_STG0_EXT_REFCLK_P
PCIE_STG0_EXT_REFCLK_N
PCIE_STG0_REXT
PCIE_STG1_TX0_P
PCIE_STG1_TX0_N
PCIE_STG1_RX0_P
PCIE_STG1_RX0_N
PCIE_STG1_TX1_P
PCIE_STG1_TX1_N
PCIE_STG1_RX1_P
PCIE_STG1_RX1_N
PCIE_STG1_TX2_P
PCIE_STG1_TX2_N
PCIE_STG1_RX2_P
PCIE_STG1_RX2_N
PCIE_STG1_TX3_P
PCIE_STG1_TX3_N
PCIE_STG1_RX3_P
PCIE_STG1_RX3_N
PCIE_STG1_REFCLK01_P
PCIE_STG1_REFCLK01_N
PCIE_STG1_CLKREQ0*
PCIE_STG1_CLKREQ1*
PCIE_STG1_REFCLK23_P
PCIE_STG1_REFCLK23_N
PCIE_STG1_CLKREQ2*
PCIE_STG1_CLKREQ3*
PCIE_STG1_PERST*
PCIE_STG1_NANDCLK
PCIE_STG1_EXT_REFCLK_P
PCIE_STG1_EXT_REFCLK_N
PCIE_STG1_REXT
PCIE_SSD1_R2D_C_P<0>
PCIE_SSD1_R2D_C_N<0>
PCIE_SSD1_D2R_P<0>
PCIE_SSD1_D2R_N<0>
PCIE_SSD1_R2D_C_P<1>
PCIE_SSD1_R2D_C_N<1>
PCIE_SSD1_D2R_P<1>
PCIE_SSD1_D2R_N<1>
PCIE_SSD1_R2D_C_P<2>
PCIE_SSD1_R2D_C_N<2>
PCIE_SSD1_D2R_P<2>
PCIE_SSD1_D2R_N<2>
PCIE_SSD1_R2D_C_P<3>
PCIE_SSD1_R2D_C_N<3>
PCIE_SSD1_D2R_P<3>
PCIE_SSD1_D2R_N<3>
PCIE_CLK100M_SSD1_01_P
PCIE_CLK100M_SSD1_01_N
SSD1_CLKREQ0_L
SSD1_CLKREQ1_L
PCIE_CLK100M_SSD1_23_P
PCIE_CLK100M_SSD1_23_N
SSD1_CLKREQ2_L
SSD1_CLKREQ3_L
SSD1_PCIE_RESET_L
SSD1_CLK24M_R
SOC_PCIE_STG0_REXT
R4250 3.01K
SOC_PCIE_STG1_REXT
R4251 3.01K
PP1V8_AWAKE
R4232 47K
ENET_CLKREQ_L
BOM_COST_GROUP=SOC
SYNC_MASTER=
SYNC_DATE=01/17/2019
PAGE TITLE
SoC PCIe
Apple Inc.
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OMIT_TABLE
CRITICAL

U3900
H9M
BGA
SYM 10 OF 18

80 PPVDDCPU_AWAKE
0.625V - 1.06V
12.5A Max

C4300 9.1UF 20% 4V CERM 0402-THICKSTNCL
C4301 9.1UF 20% 4V CERM 0402-THICKSTNCL
C4302 9.1UF 20% 4V CERM 0402-THICKSTNCL
C4303 9.1UF 20% 4V CERM 0402-THICKSTNCL
C4304 9.1UF 20% 4V CERM 0402-THICKSTNCL
C4305 9.1UF 20% 4V CERM 0402-THICKSTNCL
C4306 9.1UF 20% 4V CERM 0402-THICKSTNCL
C4307 9.1UF 20% 4V CERM 0402-THICKSTNCL
C4308 9.1UF 20% 4V CERM 0402-THICKSTNCL
C4309 9.1UF 20% 4V CERM 0402-THICKSTNCL
C4320 4.3UF 20% 4V CERM 0402-THICKSTNCL
C4321 4.3UF 20% 4V CERM 0402-THICKSTNCL
C4322 4.3UF 20% 4V CERM 0402-THICKSTNCL
C4323 4.3UF 20% 4V CERM 0402-THICKSTNCL
C4324 4.3UF 20% 4V CERM 0402-THICKSTNCL
C4330 4.3UF 20% 4V CERM 0402-THICKSTNCL
C4331 4.3UF 20% 4V CERM 0402-THICKSTNCL
C4332 4.3UF 20% 4V CERM 0402-THICKSTNCL
C4333 4.3UF 20% 4V CERM 0402-THICKSTNCL
C4334 4.3UF 20% 4V CERM 0402-THICKSTNCL

AA12	VDD_CPU	VDD_CPU_SRAM	AA10
AA14	VDD_CPU	VDD_CPU_SRAM	AB17
AA16	VDD_CPU	VDD_CPU_SRAM	AC10
AB11	VDD_CPU	VDD_CPU_SRAM	R10
AB13	VDD_CPU	VDD_CPU_SRAM	T17
AB15	VDD_CPU	VDD_CPU_SRAM	U10
AC12	VDD_CPU	VDD_CPU_SRAM	V11
AC14	VDD_CPU	VDD_CPU_SRAM	V13
AC16	VDD_CPU	VDD_CPU_SRAM	V15
AD11	VDD_CPU	VDD_CPU_SRAM	W10
AD13	VDD_CPU	VDD_CPU_SRAM	Y11
AD15	VDD_CPU	VDD_CPU_SRAM	Y13
AD17	VDD_CPU	VDD_CPU_SRAM	Y15
AE10	VDD_CPU		
AE12	VDD_CPU		
AE14	VDD_CPU		
AE16	VDD_CPU		
AE18	VDD_CPU		
P11	VDD_CPU		
P13	VDD_CPU		
P15	VDD_CPU		
P17	VDD_CPU		
R12	VDD_CPU		
R14	VDD_CPU		
R16	VDD_CPU		
T11	VDD_CPU		
T13	VDD_CPU		
T15	VDD_CPU		
U12	VDD_CPU		
U14	VDD_CPU		
U16	VDD_CPU		
V17	VDD_CPU		
W12	VDD_CPU		
W14	VDD_CPU		
W16	VDD_CPU		
Y17	VDD_CPU		
		VDD_CPU_SENSE	N18
		VSS_CPU_SENSE	N17

VDD_CPU_SENSE N18 SOC_VDDCPU_SENSE OUT 47 77
VSS_CPU_SENSE N17 NC_SOC_VSSCPU_SENSE 47

PPVDDCPUSRAM_AWAKE 80
0.8V - 1.06V
0.9A Max

C4350 9.1UF 20% 4V CERM 0402-THICKSTNCL
C4351 9.1UF 20% 4V CERM 0402-THICKSTNCL
C4352 9.1UF 20% 4V CERM 0402-THICKSTNCL
C4353 9.1UF 20% 4V CERM 0402-THICKSTNCL
C4354 9.1UF 20% 4V CERM 0402-THICKSTNCL
C4357 9.1UF 20% 4V CERM 0402-THICKSTNCL
C4355 4.3UF 20% 4V CERM 0402-THICKSTNCL
C4356 4.3UF 20% 4V CERM 0402-THICKSTNCL
C4360 4.3UF 20% 4V CERM 0402-THICKSTNCL

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OMIT_TABLE
CRITICAL

U3900
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88 PP0V82_SLPDDR
3.93A Max

C4370 9.1UF 20% 4V CERM 0402-THICKSTNCL
C4371 9.1UF 20% 4V CERM 0402-THICKSTNCL
C4372 9.1UF 20% 4V CERM 0402-THICKSTNCL
C4373 9.1UF 20% 4V CERM 0402-THICKSTNCL
C4380 4.3UF 20% 4V CERM 0402-THICKSTNCL
C4381 4.3UF 20% 4V CERM 0402-THICKSTNCL
C4385 4.3UF 20% 4V CERM 0402-THICKSTNCL
C4386 4.3UF 20% 4V CERM 0402-THICKSTNCL

AA20	VDD_SOC	VDD_SOC	J22
AA22	VDD_SOC	VDD_SOC	J24
AA24	VDD_SOC	VDD_SOC	J26
AA26	VDD_SOC	VDD_SOC	J28
AA28	VDD_SOC	VDD_SOC	L10
AC18	VDD_SOC	VDD_SOC	L12
AC20	VDD_SOC	VDD_SOC	L14
AC22	VDD_SOC	VDD_SOC	L16
AC24	VDD_SOC	VDD_SOC	L18
AC26	VDD_SOC	VDD_SOC	L20
AC28	VDD_SOC	VDD_SOC	L22
AE20	VDD_SOC	VDD_SOC	L24
AE22	VDD_SOC	VDD_SOC	L26
AE24	VDD_SOC	VDD_SOC	L28
AE26	VDD_SOC	VDD_SOC	N10
AE28	VDD_SOC	VDD_SOC	N12
AG10	VDD_SOC	VDD_SOC	N14
AG12	VDD_SOC	VDD_SOC	N16
AG14	VDD_SOC	VDD_SOC	N20
AG16	VDD_SOC	VDD_SOC	N22
AG18	VDD_SOC	VDD_SOC	N24
AG20	VDD_SOC	VDD_SOC	N26
AG22	VDD_SOC	VDD_SOC	N28
AG24	VDD_SOC	VDD_SOC	R18
AG26	VDD_SOC	VDD_SOC	R20
AG28	VDD_SOC	VDD_SOC	R22
AJ10	VDD_SOC	VDD_SOC	R24
AJ12	VDD_SOC	VDD_SOC	R26
AJ14	VDD_SOC	VDD_SOC	R28
AJ16	VDD_SOC	VDD_SOC	U18
AJ18	VDD_SOC	VDD_SOC	U20
AJ20	VDD_SOC	VDD_SOC	U22
AJ22	VDD_SOC	VDD_SOC	U24
AJ24	VDD_SOC	VDD_SOC	U26
AJ26	VDD_SOC	VDD_SOC	U28
AJ28	VDD_SOC	VDD_SOC	W20
J10	VDD_SOC	VDD_SOC	W22
J12	VDD_SOC	VDD_SOC	W24
J14	VDD_SOC	VDD_SOC	W26
J16	VDD_SOC	VDD_SOC	W28
J18	VDD_SOC		
J20	VDD_SOC		
		VDD_SOC_SENSE	AD27
		VSS_SENSE	AD28

VDD_SOC_SENSE AD27 SOC_VDDSOC_SENSE 47
VSS_SENSE AD28 NC_SOC_VSSSOC_SENSE 47

BOM_COST_GROUP=SOC

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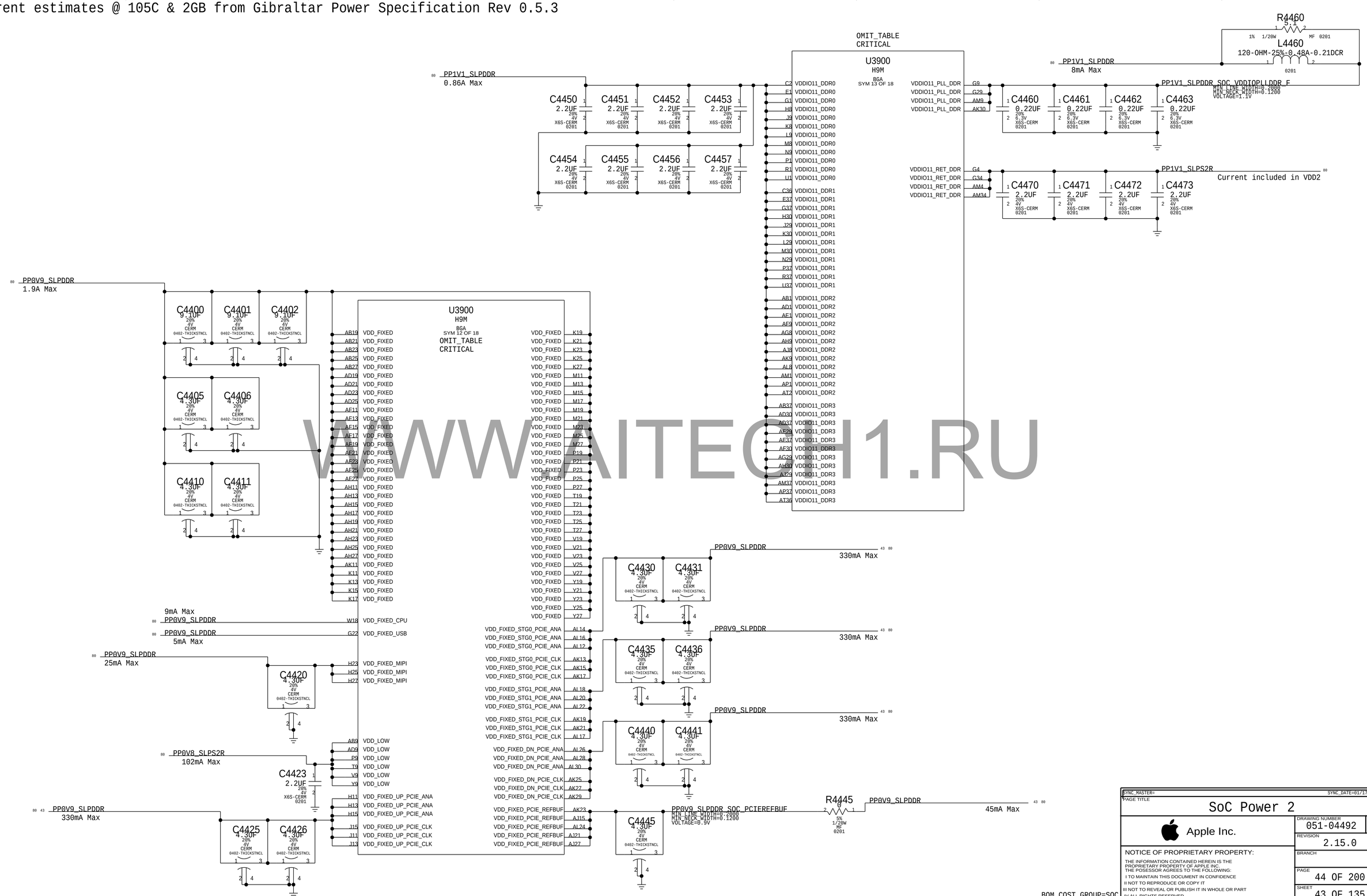

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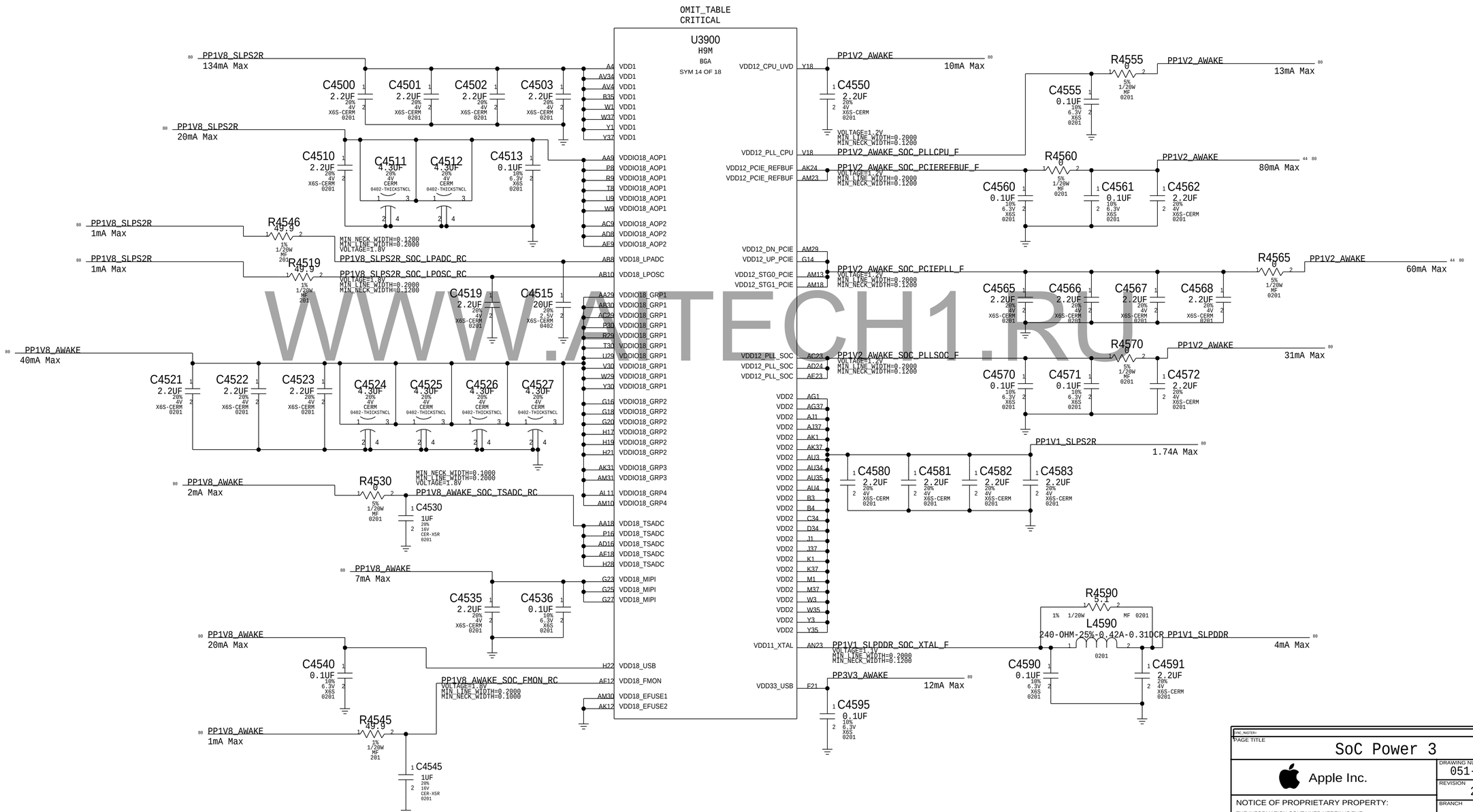

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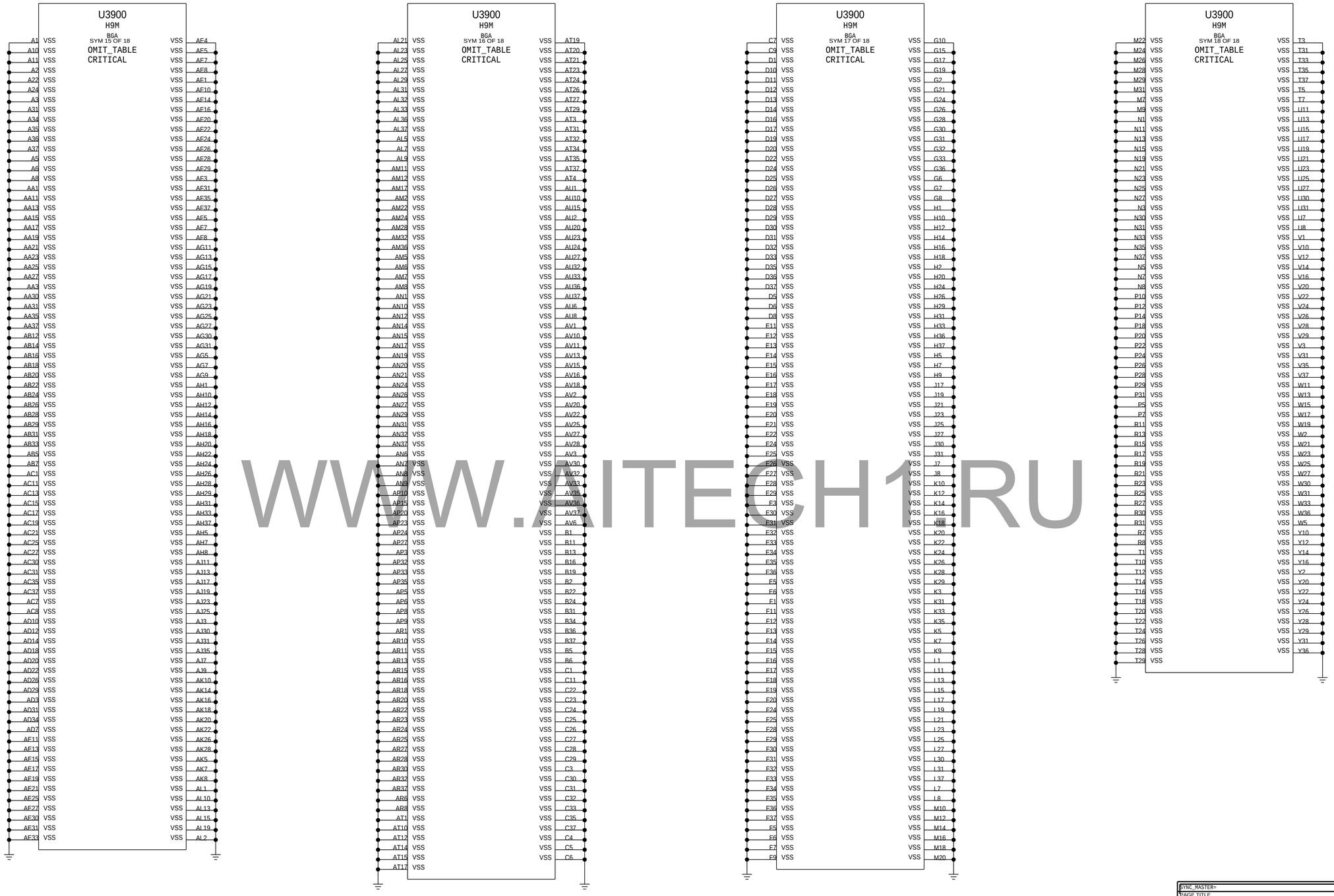

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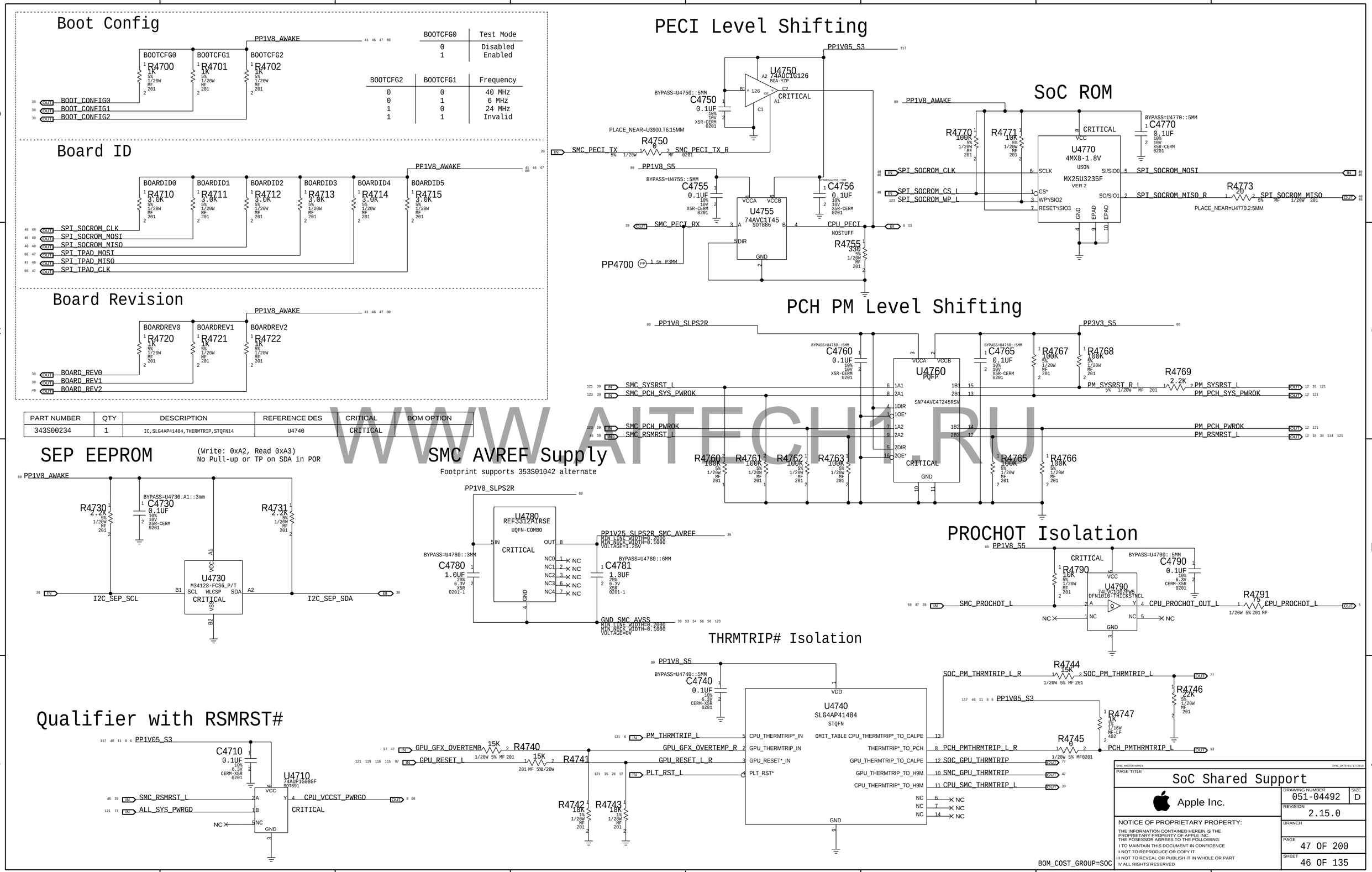

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S00234	1	IC,SLG4AP41484,THERMTRIP,STQFN14	U4740	CRITICAL	

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* Tentative	BOM GROUP	BOM OPTIONS
	BOARD_REV:111	BOARDREV2,BOARDREV1,BOARDREV0
	BOARD_REV:110	BOARDREV2,BOARDREV1
	BOARD_REV:101	BOARDREV2,BOARDREV0
	BOARD_REV:100	BOARDREV2
PVT*	BOARD_REV:011	BOARDREV1,BOARDREV0
EVT*	BOARD_REV:010	BOARDREV1
Proto 3	BOARD_REV:001	BOARDREV0
Proto 0a	BOARD_REV:000	

PCIe Up R2D AC Caps

(All Caps)

PCIE_SOC_R2D_C_P<0>	C4820	0.22UF	20%	6.3V	X5R	0201	PCIE_SOC_R2D_P<0>	OUT	41 120
PCIE_SOC_R2D_C_N<0>	C4821	0.22UF	20%	6.3V	X5R	0201	PCIE_SOC_R2D_N<0>	OUT	41 120
PCIE_SOC_R2D_C_P<1>	C4822	0.22UF	20%	6.3V	X5R	0201	PCIE_SOC_R2D_P<1>	OUT	41 120
PCIE_SOC_R2D_C_N<1>	C4823	0.22UF	20%	6.3V	X5R	0201	PCIE_SOC_R2D_N<1>	OUT	41 120
PCIE_SOC_R2D_C_P<2>	C4824	0.22UF	20%	6.3V	X5R	0201	PCIE_SOC_R2D_P<2>	OUT	41 120
PCIE_SOC_R2D_C_N<2>	C4825	0.22UF	20%	6.3V	X5R	0201	PCIE_SOC_R2D_N<2>	OUT	41 120
PCIE_SOC_R2D_C_P<3>	C4826	0.22UF	20%	6.3V	X5R	0201	PCIE_SOC_R2D_P<3>	OUT	41 120
PCIE_SOC_R2D_C_N<3>	C4827	0.22UF	20%	6.3V	X5R	0201	PCIE_SOC_R2D_N<3>	OUT	41 120

GPIO Source Termination

I2S_SPKRAMP_L_R2D_R	R4843	20	1	2	5% 1/20W MF 201	I2S_SPKRAMP_L_R2D	OUT	62
I2S_SPKRAMP_L_BCLK_R	R4844	20	1	2	5% 1/20W MF 201	I2S_SPKRAMP_L_BCLK	OUT	62
I2S_SPKRAMP_L_LRCLK_R	R4863	20	1	2	5% 1/20W MF 201	I2S_SPKRAMP_L_LRCLK	OUT	40
I2S_SPKRAMP_R_R2D_R	R4845	20	1	2	5% 1/20W MF 201	I2S_SPKRAMP_R_R2D	OUT	63
I2S_SPKRAMP_R_BCLK_R	R4846	20	1	2	5% 1/20W MF 201	I2S_SPKRAMP_R_BCLK	OUT	63
I2S_SPKRAMP_R_LRCLK_R	R4864	20	1	2	5% 1/20W MF 201	I2S_SPKRAMP_R_LRCLK	OUT	40
I2S_CODEC_R2D_R	R4847	20	1	2	5% 1/20W MF 201	I2S_CODEC_R2D	OUT	61
I2S_CODEC_BCLK_R	R4848	20	1	2	5% 1/20W MF 201	I2S_CODEC_BCLK	OUT	61
I2S_CODEC_LRCLK_R	R4865	20	1	2	5% 1/20W MF 201	I2S_CODEC_LRCLK	OUT	48
SPI_TPAD_MOSI_R	R4851	20	1	2	5% 1/20W MF 201	SPI_TPAD_MOSI	OUT	46 66
SPI_TPAD_CLK_R	R4852	20	1	2	5% 1/20W MF 201	SPI_TPAD_CLK	OUT	46 66
SPI_MESA_MOSI_R	R4853	20	1	2	5% 1/20W MF 201	SPI_MESA_MOSI	OUT	48
SPI_MESA_CLK_R	R4854	20	1	2	5% 1/20W MF 201	SPI_MESA_CLK	OUT	48
SPI_DFR_MISO_R	R4866	20	1	2	5% 1/20W MF 201	SPI_DFR_MISO	IN	48
SPI_DFR_MOSI_R	R4855	20	1	2	5% 1/20W MF 201	SPI_DFR_MOSI	OUT	50 122
SPI_DFR_CLK_R	R4856	20	1	2	5% 1/20W MF 201	SPI_DFR_CLK	OUT	50 122
SSD0_CLK24M_R	R4857	20	1	2	5% 1/20W MF 201	SSD0_CLK24M	OUT	47 88 90
SSD1_CLK24M_R	R4858	20	1	2	5% 1/20W MF 201	SSD1_CLK24M	OUT	47 83 85
PDM_DMIC_CLK0_R	R4859	20	1	2	5% 1/20W MF 201	AUD_DMIC0_CLK_CONN	OUT	64 122
PDM_DMIC_CLK1_R	R4860	20	1	2	5% 1/20W MF 201	AUD_DMIC1_CLK_CONN	OUT	64 122
SPI_AOP_SENSOR_MOSI_R	R4812	20	1	2	5% 1/20W MF 201	SPI_AOP_MA781_MOSI	OUT	47 122
SPI_AOP_SENSOR_CLK_R	R4813	20	2	1	5% 1/20W MF 201	SPI_AOP_MA781_CLK	OUT	47 122
SPI_AOP_MA781_MISO	R4811	20	2	1	5% 1/20W MF 201	SPI_AOP_SENSOR_MISO	IN	39 47
SPI_TPAD_MISO	R4809	20	1	2	5% 1/20W MF 201	SPI_TPAD_MISO_R	IN	66
SE_HOST_WAKE_R	R4807	0	2	1	5% 1/20W MF 0201	SE_HOST_WAKE	IN	49

UART_BT_LH_R2D	MAKE_BASE=TRUE	UART_BT_LH_R2D
UART_BT_LH_D2R	MAKE_BASE=TRUE	UART_BT_LH_D2R
NC_SWD_WLAN_SWDIO	MAKE_BASE=TRUE	NC_SWD_WLAN_SWDIO
NC_SWD_WLAN_SWCLK	MAKE_BASE=TRUE NO_TEST=1	NC_SWD_WLAN_SWCLK
WLAN_JTAG_TDI	MAKE_BASE=TRUE	WLAN_JTAG_TDI
NC_SMC_LED_ONEWIRE	MAKE_BASE=TRUE NO_TEST=1	NC_SMC_LED_ONEWIRE
NC_WLAN_CONTEXT_B	MAKE_BASE=TRUE	NC_WLAN_CONTEXT_B

No Connects

NC_GYRO_INT1	MAKE_BASE=TRUE NO_TEST=1	NC_GYRO_INT1	
NC_GYRO_INT2	MAKE_BASE=TRUE NO_TEST=1	NC_GYRO_INT2	
NC_SPI_GYRO_CS_L	MAKE_BASE=TRUE NO_TEST=1	NC_SPI_GYRO_CS_L	
SPI_AOP_MA781_CS_L	MAKE_BASE=TRUE	SPI_AOP_MA781_CS_L	47 122
NC_ALTIMETER_INT	MAKE_BASE=TRUE NO_TEST=1	NC_ALTIMETER_INT	
NC_PMU_CLK32K_GNSS_R	MAKE_BASE=TRUE NO_TEST=1	NC_PMU_CLK32K_GNSS_R	
NC_LIDOPEN_PSU12VPGOOD_ACDCBURST_L	MAKE_BASE=TRUE	NC_LIDOPEN_PSU12VPGOOD_ACDCBURST_L	
LID_OPEN_SMC_IN	MAKE_BASE=TRUE	LID_OPEN_SMC_IN	47
NC_UART_GNSS_D2R_CTS_L	MAKE_BASE=TRUE	NC_UART_GNSS_D2R_CTS_L	
NC_UART_GNSS_R2D_RTS_L	MAKE_BASE=TRUE	NC_UART_GNSS_R2D_RTS_L	
NC_GNSS_HOST_TIME	MAKE_BASE=TRUE	NC_GNSS_HOST_TIME	
NC_GNSS_HOST_WAKE	MAKE_BASE=TRUE	NC_GNSS_HOST_WAKE	
NC_GNSS_DEV_WAKE	MAKE_BASE=TRUE	NC_GNSS_DEV_WAKE	
NC_ENET_MEDIA_SENSE	MAKE_BASE=TRUE	NC_ENET_MEDIA_SENSE	
NC_ENET_LOW_PWR	MAKE_BASE=TRUE	NC_ENET_LOW_PWR	
NC_I2S_HAWKING_D2R	MAKE_BASE=TRUE	NC_I2S_HAWKING_D2R	
NC_I2S_HAWKING_LRCLK	MAKE_BASE=TRUE	NC_I2S_HAWKING_LRCLK	
NC_I2S_HAWKING_BCLK	MAKE_BASE=TRUE	NC_I2S_HAWKING_BCLK	
NC_I2S_CODEC1_R2D_R	MAKE_BASE=TRUE	NC_I2S_CODEC1_R2D_R	
NC_PLCAM_RX_CLK12M_R	MAKE_BASE=TRUE	NC_PLCAM_RX_CLK12M_R	
NC_PLCAM_RX_RESET_L	MAKE_BASE=TRUE	NC_PLCAM_RX_RESET_L	
NC_PLCAM_TX_CLK12M_R	MAKE_BASE=TRUE	NC_PLCAM_TX_CLK12M_R	
NC_PLCAM_TX_RESET_L	MAKE_BASE=TRUE	NC_PLCAM_TX_RESET_L	
NC_PLCAM_TX_INT	MAKE_BASE=TRUE	NC_PLCAM_TX_INT	
NC_PLCAM_TX_THROTTLE	MAKE_BASE=TRUE	NC_PLCAM_TX_THROTTLE	
NC_PLCAM_PROX_INT_L	MAKE_BASE=TRUE	NC_PLCAM_PROX_INT_L	
NC_PLCAM_ROMEO_B2B_DETECT	MAKE_BASE=TRUE	NC_PLCAM_ROMEO_B2B_DETECT	
NC_PCHROM_SW_EN	MAKE_BASE=TRUE	NC_PCHROM_SW_EN	
NC_SDCONN_STATE_CHANGE_L	MAKE_BASE=TRUE	NC_SDCONN_STATE_CHANGE_L	
NC_FTCAM_RESET_L	MAKE_BASE=TRUE	NC_FTCAM_RESET_L	
NC_FTCAM_CLK12M_R	MAKE_BASE=TRUE	NC_FTCAM_CLK12M_R	
NC_I2S_CODEC_MCLK	MAKE_BASE=TRUE	NC_I2S_CODEC_MCLK	
NC_I2S_CODEC1_MCLK	MAKE_BASE=TRUE	NC_I2S_CODEC1_MCLK	
NC_SPI_DESCRIPTOR_OVERRIDE_L	MAKE_BASE=TRUE	NC_SPI_DESCRIPTOR_OVERRIDE_L	
NC_I2C_AOP_SCL	MAKE_BASE=TRUE	NC_I2C_AOP_SCL	
NC_I2C_AOP_SDA	MAKE_BASE=TRUE	NC_I2C_AOP_SDA	
NC_SOC_USB_ID	MAKE_BASE=TRUE	NC_SOC_USB_ID	
NC_SOC_AMUXOUT	MAKE_BASE=TRUE	NC_SOC_AMUXOUT	
NC_SPKR_ID1	MAKE_BASE=TRUE	NC_SPKR_ID1	
NC_SPKR_ID0	MAKE_BASE=TRUE	NC_SPKR_ID0	
NC_PCIEDN_WAKE_L	MAKE_BASE=TRUE	NC_PCIEDN_WAKE_L	
NC_MESA_MENUKEY_L	MAKE_BASE=TRUE	NC_MESA_MENUKEY_L	
NC_AUD_PWR_EN	MAKE_BASE=TRUE	NC_AUD_PWR_EN	
NC_PCIE_CLK100M_DN2P	MAKE_BASE=TRUE	NC_PCIE_CLK100M_DN2P	
NC_PCIE_CLK100M_DN2N	MAKE_BASE=TRUE	NC_PCIE_CLK100M_DN2N	
NC_PCIEDN2_CLKREQ_L	MAKE_BASE=TRUE	NC_PCIEDN2_CLKREQ_L	
NC_PCIEDN2_RESET_L	MAKE_BASE=TRUE	NC_PCIEDN2_RESET_L	
NC_UART_BT_R2D	MAKE_BASE=TRUE	NC_UART_BT_R2D	
NC_UART_BT_D2R	MAKE_BASE=TRUE	NC_UART_BT_D2R	
NC_UART_BT_R2D_RTS_L	MAKE_BASE=TRUE	NC_UART_BT_R2D_RTS_L	
NC_UART_BT_D2R_CTS_L	MAKE_BASE=TRUE	NC_UART_BT_D2R_CTS_L	
NC_PCIE_DN2_R2D_CP	MAKE_BASE=TRUE	NC_PCIE_DN2_R2D_CP	
NC_PCIE_DN2_R2D_CN	MAKE_BASE=TRUE	NC_PCIE_DN2_R2D_CN	
NC_PCIE_DN2_D2RP	MAKE_BASE=TRUE	NC_PCIE_DN2_D2RP	
NC_PCIE_DN2_D2RN	MAKE_BASE=TRUE	NC_PCIE_DN2_D2RN	
NC_TPAD_ACTUATOR_DISABLE_L	MAKE_BASE=TRUE	NC_TPAD_ACTUATOR_DISABLE_L	
NC_WLAN_CONTEXT_A	MAKE_BASE=TRUE NO_TEST=1	NC_WLAN_CONTEXT_A	

NC_WLAN_CLKREQ_L	MAKE_BASE=TRUE	NC_WLAN_CLKREQ_L	
NC_WLAN_PERST_L	MAKE_BASE=TRUE	NC_WLAN_PERST_L	
NC_PCIE_ENET_R2D_C_P	MAKE_BASE=TRUE	NC_PCIE_ENET_R2D_C_P	
NC_PCIE_ENET_R2D_C_N	MAKE_BASE=TRUE	NC_PCIE_ENET_R2D_C_N	
NC_PCIE_ENET_D2R_P	MAKE_BASE=TRUE	NC_PCIE_ENET_D2R_P	
NC_PCIE_ENET_D2R_N	MAKE_BASE=TRUE	NC_PCIE_ENET_D2R_N	
NC_PCIE_CLK100M_ENET_P	MAKE_BASE=TRUE	NC_PCIE_CLK100M_ENET_P	
NC_PCIE_CLK100M_ENET_N	MAKE_BASE=TRUE	NC_PCIE_CLK100M_ENET_N	
NC_PCIE_CLK100M_WLAN_P	MAKE_BASE	NC_PCIE_CLK100M_WLAN_P	
NC_PCIE_CLK100M_WLAN_N	MAKE_BASE	NC_PCIE_CLK100M_WLAN_N	
NC_PCIE_DN3_R2D_CN	MAKE_BASE=TRUE	NC_PCIE_DN3_R2D_CN	
NC_PCIE_DN3_D2RP	MAKE_BASE=TRUE	NC_PCIE_DN3_D2RP	
NC_PCIE_DN3_D2RN	MAKE_BASE=TRUE	NC_PCIE_DN3_D2RN	
NC_PCIE_CLK100M_DN3P	MAKE_BASE=TRUE	NC_PCIE_CLK100M_DN3P	
NC_PCIE_CLK100M_DN3N	MAKE_BASE=TRUE	NC_PCIE_CLK100M_DN3N	
NC_PCIEDN3_CLKREQ_L	MAKE_BASE=TRUE	NC_PCIEDN3_CLKREQ_L	
NC_PCIEDN3_RESET_L	MAKE_BASE=TRUE	NC_PCIEDN3_RESET_L	
NC_PCIE_WLAN_R2D_C_P	MAKE_BASE=TRUE	NC_PCIE_WLAN_R2D_C_P	
NC_PCIE_WLAN_R2D_C_N	MAKE_BASE=TRUE	NC_PCIE_WLAN_R2D_C_N	
NC_PCIE_WLAN_D2R_P	MAKE_BASE=TRUE	NC_PCIE_WLAN_D2R_P	
NC_PCIE_WLAN_D2R_N	MAKE_BASE=TRUE	NC_PCIE_WLAN_D2R_N	
NC_SOC_VSSCPU_SENSE	MAKE_BASE=TRUE	NC_SOC_VSSCPU_SENSE	
NC_SOC_VSSSOC_SENSE	MAKE_BASE=TRUE	NC_SOC_VSSSOC_SENSE	
NC_DFR_TOUCH_RSVD	MAKE_BASE=TRUE	NC_DFR_TOUCH_RSVD	
NC_PCIE_DN3_R2D_CP	MAKE_BASE=TRUE	NC_PCIE_DN3_R2D_CP	
NC_TPAD_VIBE_L	MAKE_BASE=TRUE	NC_TPAD_VIBE_L	
NC_ENET_RESET_L	MAKE_BASE=TRUE	NC_ENET_RESET_L	
NC_WLAN_DEV_WAKE	MAKE_BASE=TRUE	NC_WLAN_DEV_WAKE	

PP1V8_G3S								49 118 121 122
PP1V8_SLPS2R								38 80
PP1V8_AWAKE								41 46 80
R4883	47K	1	2	5% 1/20W MF 201	SSD0_CLKREQ0_L			41 88 123
R4884	47K	1	2	5% 1/20W MF 201	SSD0_CLKREQ1_L			41 89 123
R4887	47K	1	2	5% 1/20W MF 201	SSD0_CLKREQ2_L			41 90 123
R4888	47K	1	2	5% 1/20W MF 201	SSD0_CLKREQ3_L			41 91 123
R4889	47K	1	2	5% 1/20W MF 201	SSD1_CLKREQ0_L			41 83
R4890	47K	1	2	5% 1/20W MF 201	SSD1_CLKREQ1_L			41 84 123
R4891	47K	1	2	5% 1/20W MF 201	SSD1_CLKREQ2_L			41 85
R4892	47K	1	2	5% 1/20W MF 201	SSD1_CLKREQ3_L			41 86
R4895	100K	1	2	5% 1/20W MF 201	SSD_PMU_RESET_L			38 87 92 121
R3611	100K	1	2	5% 1/20W MF 201	SPI_AOP_SENSOR_MOSI_R			39 47
R3612	100K	1	2	5% 1/20W MF 201	SPI_AOP_SENSOR_CLK_R			39 47
R3613	100K	1	2	5% 1/20W MF 201	SPI_AOP_SENSOR_MISO			39 47
R4820	100K	1	2	5% 1/20W MF 201	SPI_AOP_MA781_CS_L			47 122
R4885	100K	1	2	5% 1/20W MF 201	SSD0_PCIE_RESET_L			41 88 89 90 91
R4886	47K	1	2	5% 1/20W MF 201	SSD0_CLK24M			47 88 90
R4893	100K	1	2	5% 1/20W MF 201	SSD1_PCIE_RESET_L			41 83 84 85 86
R4894	47K	1	2	5% 1/20W MF 201	SSD1_CLK24M			47 83 85
R4870	0	1	2	5% 1/20W MF 0201	I2S_SPKRAMP_R_D2R			40

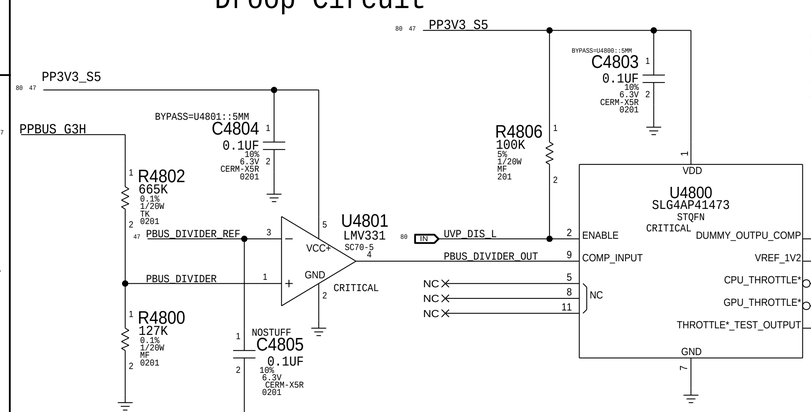
42	IN	SOC_VDDSOC_SENSE	P3MM SM 1	PP4800
77 42	IN	SOC_VDDCPU_SENSE	P3MM SM 1	PP4801
92 91 90 89 88	IN	SSD0_OCARINA_WP_L	P5MM-SP SM-SP 1	PP4802
87 86 85 84 83	IN	SSD1_OCARINA_WP_L	P5MM-SP SM-SP 1	PP4803
69 47 46 39	IN	SMC_PROCHOT_L	P3MM SM 1	PP4808
77 68	IN	CHGR_INT_L PLACE_SIDE=BOTTOM	SM P2MM 1	PP4809
122 47	IN	ANGLE_SENSOR_MGL PLACE_SIDE=BOTTOM	SM P2MM	PP4810

INT PU SOC 50k

39 SMC_FIXTURE_MODE_L — 121 SMC_FIXTURE_MODE_L (MAKE_BASE)

FIXMODE_NO R4801 100K 5% 1/20W MF 201

Droop Circuit

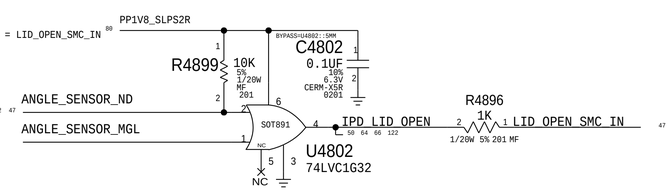


Signal Aliases

TPAD_KBD_WAKE_L	MAKE_BASE	TPAD_KBD_WAKE_L	66 122
TPAD_SPI_INT_L	MAKE_BASE	TPAD_SPI_INT_L	66
GPU_GFX_OVERTEMP	MAKE_BASE	GPU_GFX_OVERTEMP	46 97
SMC_GPU_THRMTRIP	MAKE_BASE	SMC_GPU_THRMTRIP	46
SOC_KBD_BKLT_PWM	MAKE_BASE	SOC_KBD_BKLT_PWM	81

GND	MAKE_BASE	
GND	MAKE_BASE	
GND	MAKE_BASE	
GND	MAKE_BASE	
GND	MAKE_BASE	
GND	MAKE_BASE	
GND	MAKE_BASE	
GND	MAKE_BASE	

Note
GPIO4 = LID_OPEN_SMC_IN



Lid Detect Sensors

J4802
503548-1220
51650873
F-ST-SM

122 47	ANGLE_SENSOR_ND	PP3V3_G3H_RTC_X	118
122 47	SPI_AOP_MA781_CS_L	PP1V8_SLPS2R	80
122 47	ANGLE_SENSOR_MGL	SPI_AOP_MA781_MISO	47 122
122 47	SPI_AOP_MA781_CLK	SPI_AOP_MA781_MOSI	47 122

C4830 1.0UF 20% 6.3V X5R 0201-1 (BYPASS=J4802::5MM)
C4831 1.0UF 20% 6.3V X5R 0201-1 (BYPASS=J4802::5MM)

BOM_COST_GROUP=SOC

PAGE TITLE: SoC Project Support

Apple Inc.

DRAWING NUMBER: 051-04492 SIZE: D
REVISION: 2.15.0
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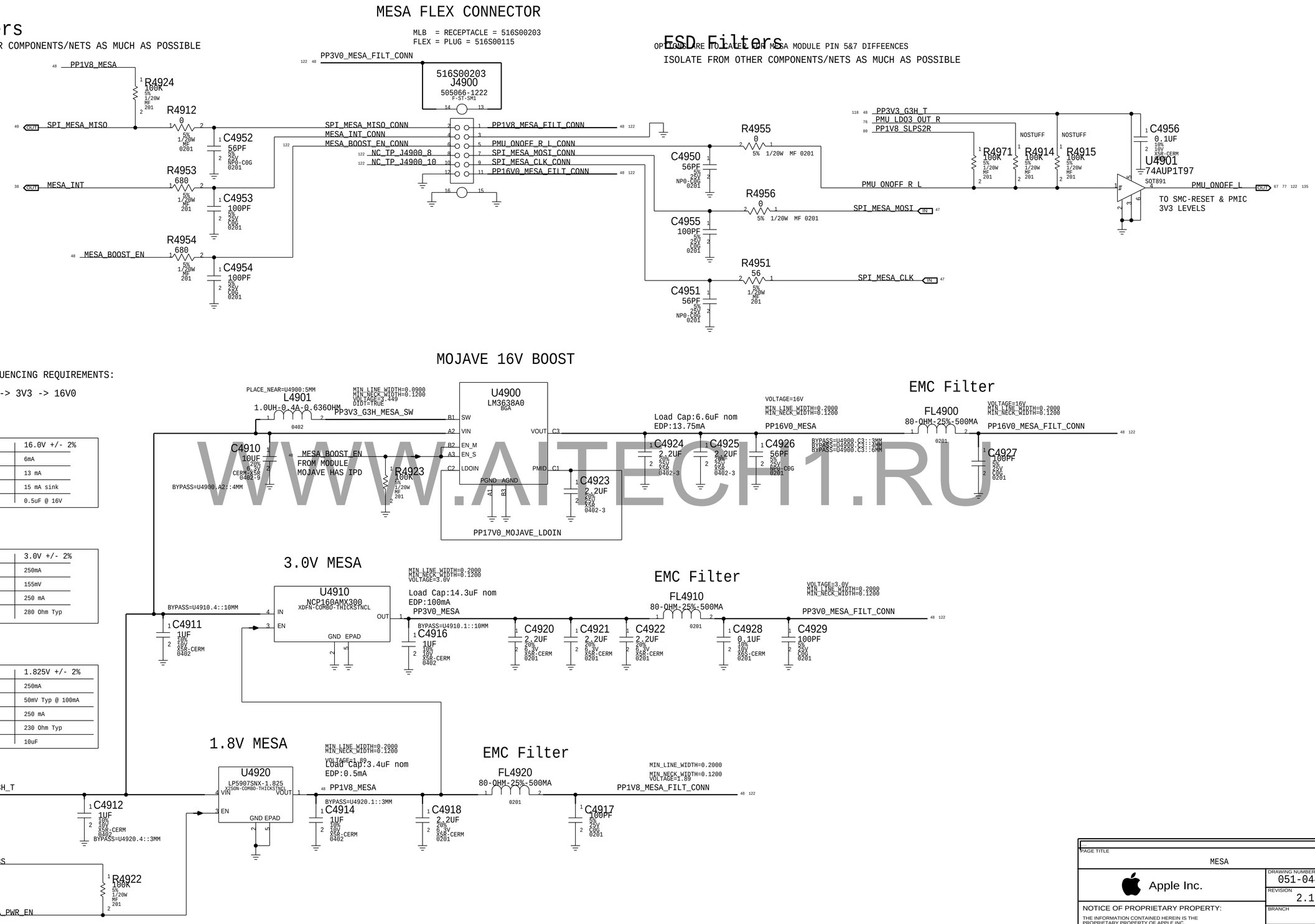

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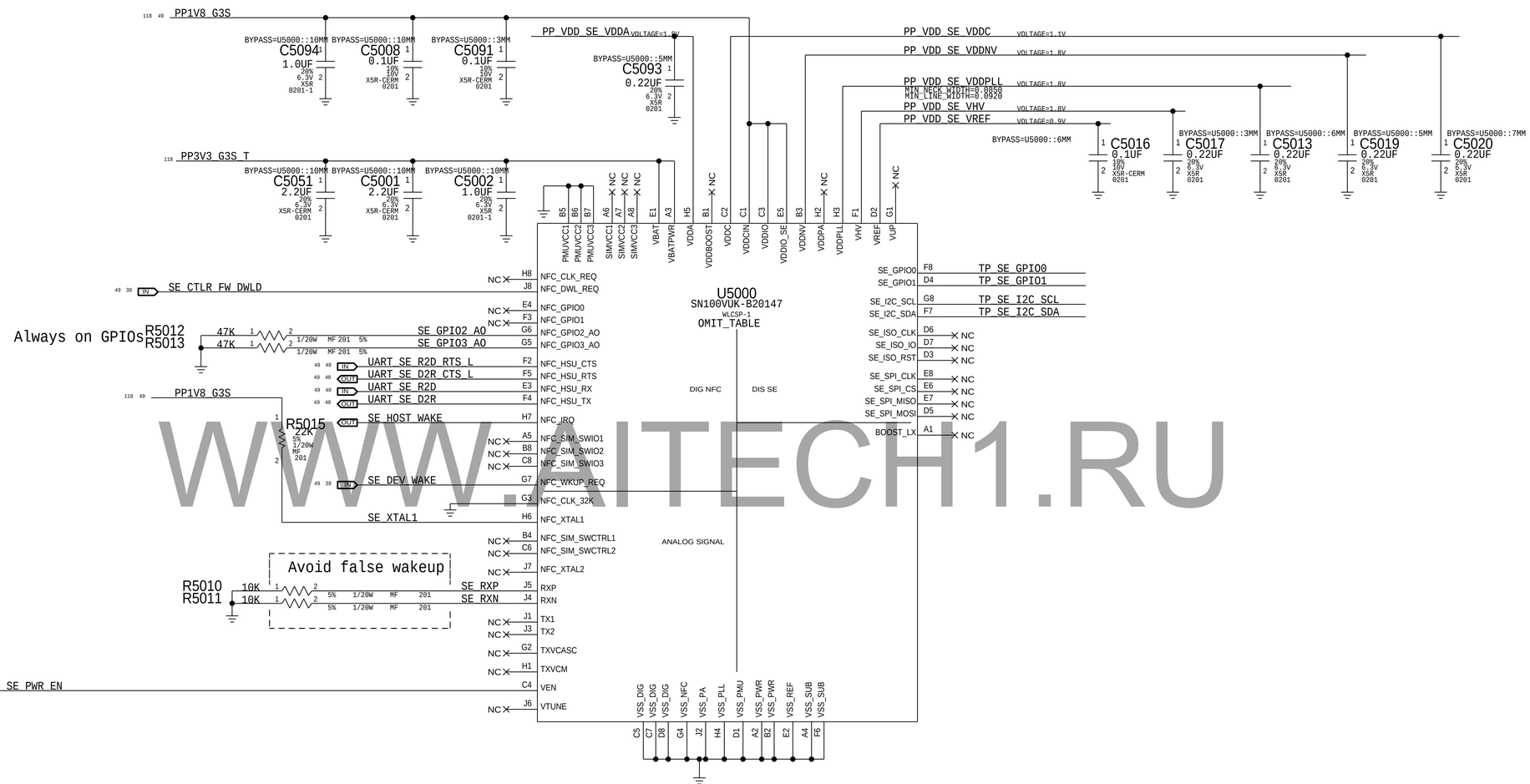
VENUS



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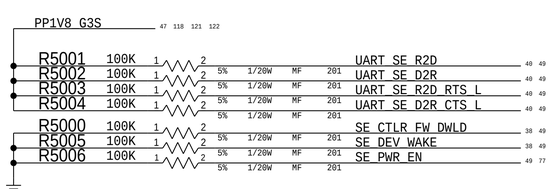

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-15216	1	IC,SN100V,DEV,B2,WLCSP72	U5000	CRITICAL	SE:DEV_2019
338S00445	1	IC,SN100V,PROD,B2,WLCSP72	U5000	CRITICAL	SE:PROD_2019

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PAGE TITLE
SECURE ELEMENT

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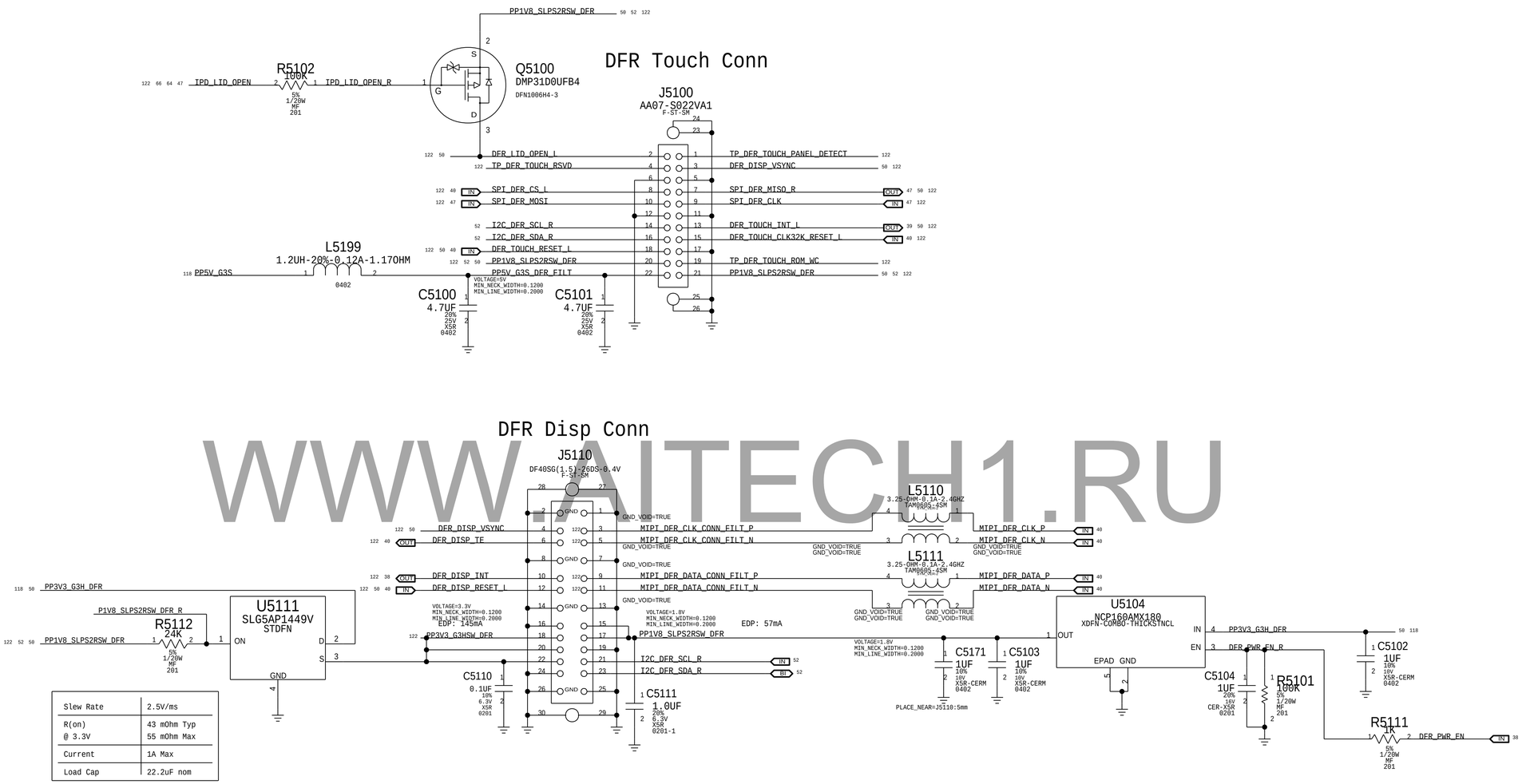
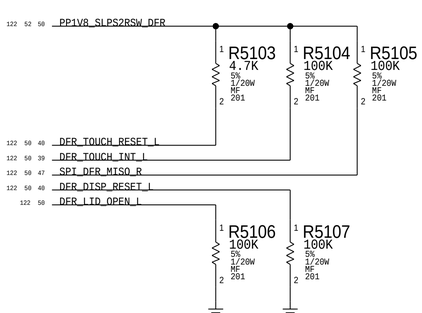


Slew Rate	2.5V/ms
R(on) @ 3.3V	43 mOhm Typ 55 mOhm Max
Current	1A Max
Load Cap	22.2uF nom



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BOM_COST_GROUP=T151

PAGE TITLE
DFR Support

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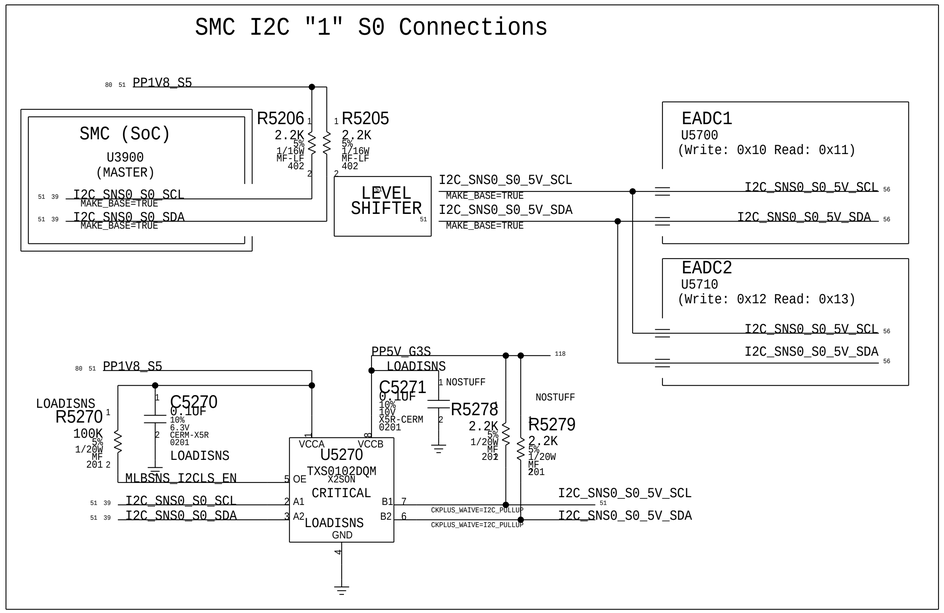

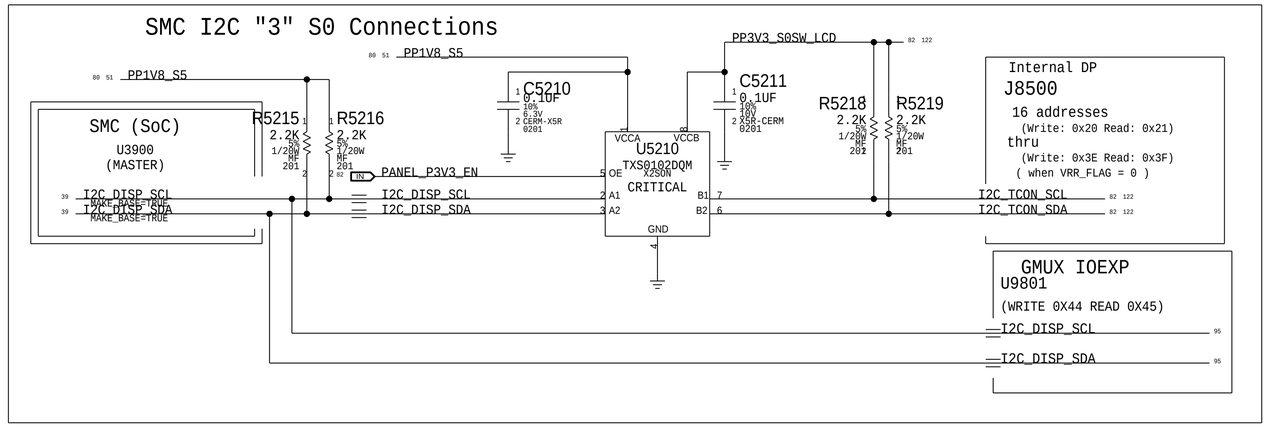

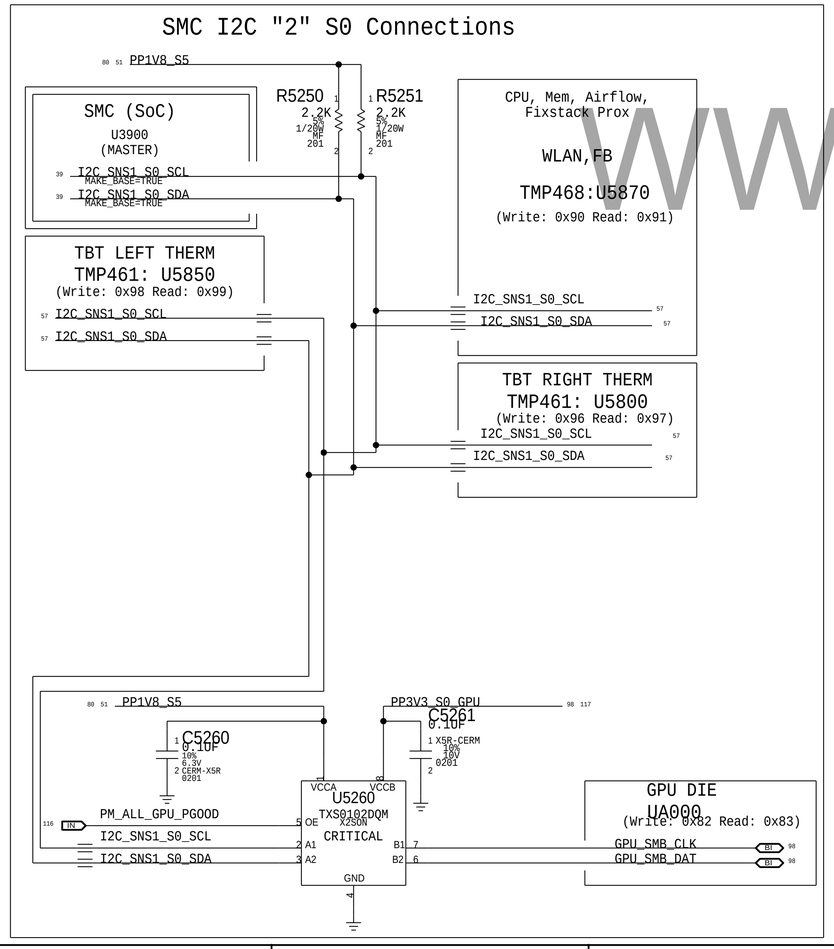

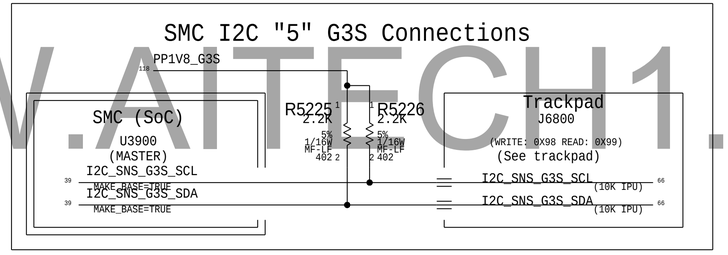

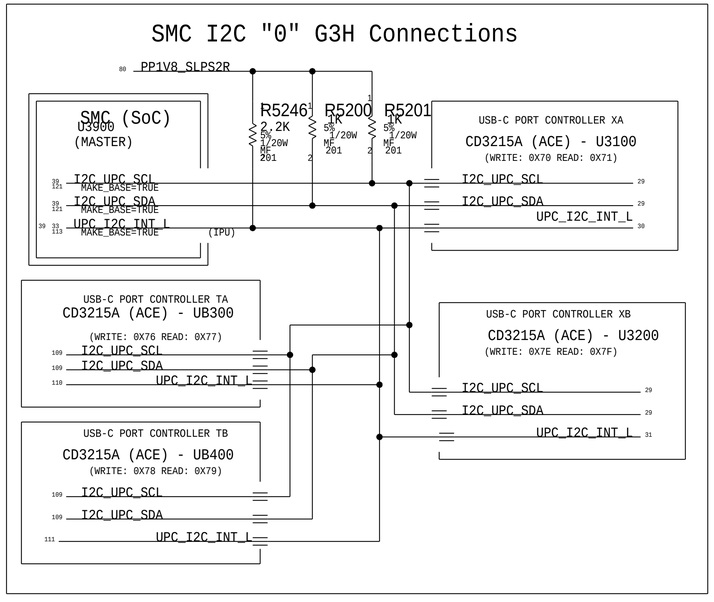

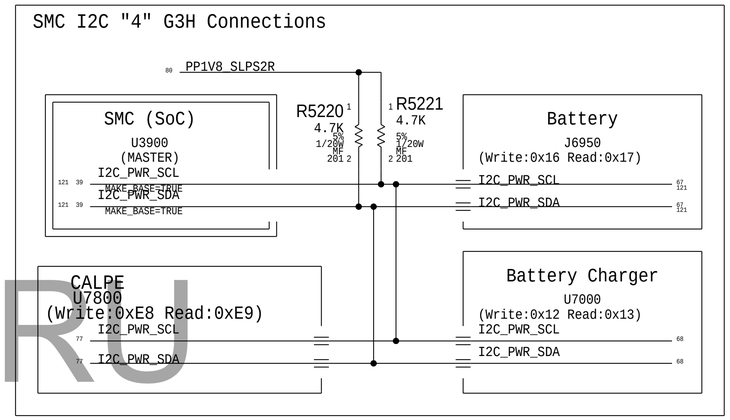

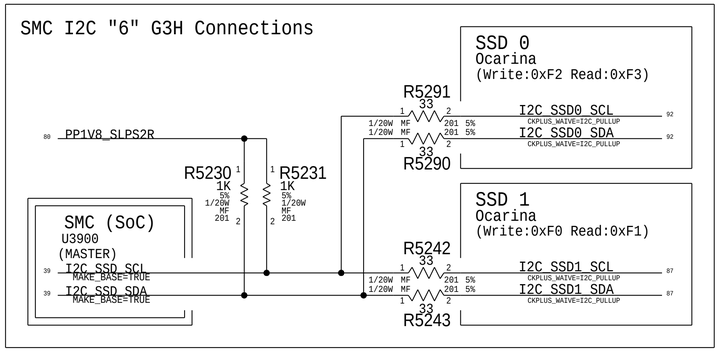

BOM_COST_GROUP=SMC

PAGE TITLE
I2C Connections 1

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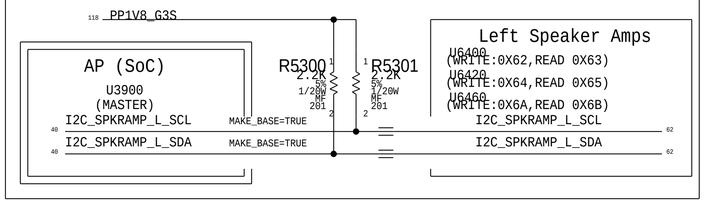
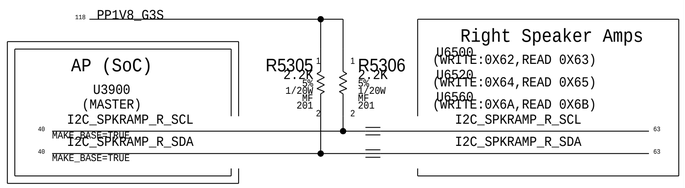
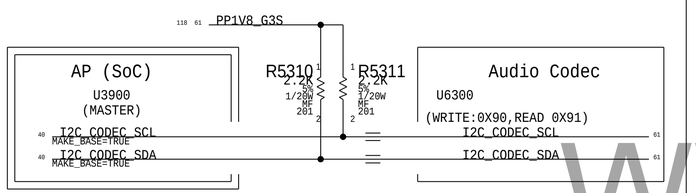
AP I2C "0" G3S Connections



AP I2C "1" G3S Connections



AP I2C "2" Codec Connections



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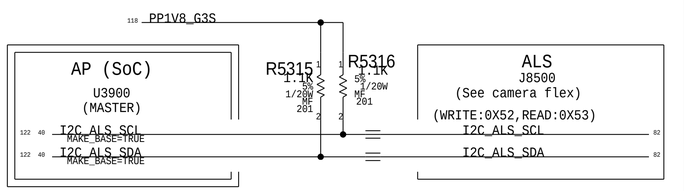
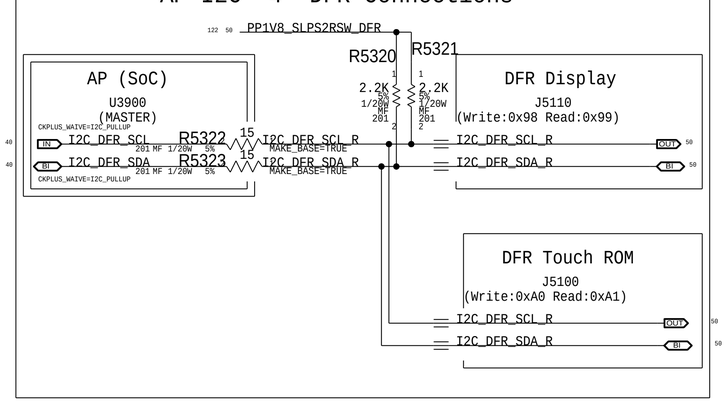
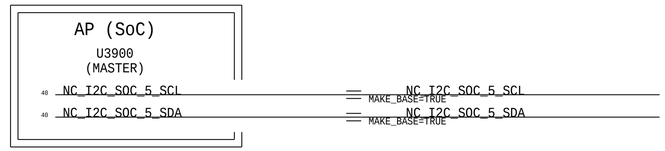


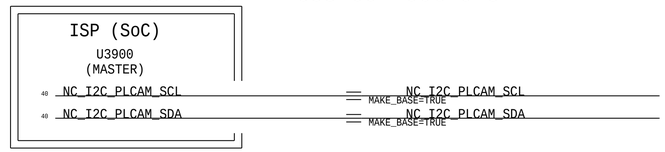
AP I2C "4" DFR Connections



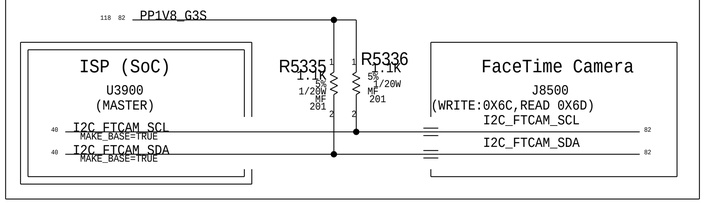
AP I2C "5" Awake Connections



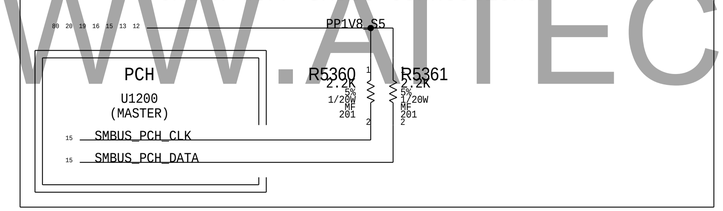
ISP I2C "1" G3S Connections



ISP I2C "0" G3S Connections



CNL-H uSFF SMBUS Connections



I2C Device Address

Device	SMC IF	ADDR. (8b)
ACE XA	I2C0	0X70/1
ACE XB	I2C0	0X7E/F
ACE TA	I2C0	0X76/7
ACE TB	I2C0	0X78/9
EADC1	I2C1	0X10/1
EADC2	I2C1	0X12/3
Temp. Sensor Left	I2C2	0X98/9
Temp. Sensor Right	I2C2	0X96/7
CPU,MEM,WLAN Thermal	I2C2	0X90/1
GPU Analog Die Thermal	I2C2	0X92/3
GPU Digital Die Thermal	I2C2	0X82/3
TCON	I2C3	0X20/1
GMUX IOEXP	I2C3	0X44/5
Charger	I2C4	0X12/3
Battery	I2C4	0X16/7
Calpe	I2C4	0XE8/9
Trackpad	I2C5	0X98/9
SSD0	I2C6	0XF2/3
SSD1	I2C6	0XF0/1
SoC IF		
Left Spkr Amp.(U6400)	I2C0	0X62/3
Left Spkr Amp.(U6420)	I2C0	0X64/5
Left Spkr Amp.(U6460)	I2C0	0X6A/B
Right Spkr Amp.(U6500)	I2C1	0X62/3
Right Spkr Amp.(U6520)	I2C1	0X63/4
Right Spkr Amp.(U6560)	I2C1	0X6A/B
Audio Codec	I2C2	0X90/1
ALS	I2C3	0X52/3
DFR Display	I2C4	0X98/9
DFR Touch	I2C4	0XA0/1
NC.	I2C5	
NC.Spkr ID1	I2C6_SDA	
NC.Spkr ID0	I2C6_SCL	
ISP IF		
FT Camera	I2C0	0X6C/D
NC.	I2C1	
AOP IF		
NC.	I2C0	
PCH IF		
NC.	PULL-UP	

BOM_COST_GROUP=SMC

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PAGE TITLE: I2C Connections 2

Apple Inc.

DRAWING NUMBER: 051-04492 SIZE: D

REVISION: 2.15.0

BRANCH:

PAGE: 53 OF 200

SHEET: 52 OF 135

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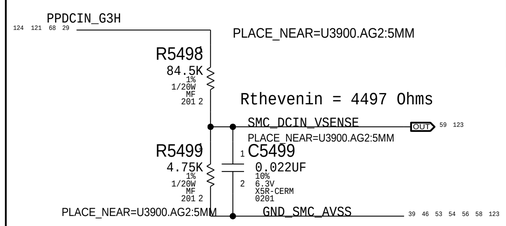
DC-IN Voltage Sense (VD0R)

Gain: 0.05322x
Vnominal: 20 V, Range: 23.49 V
SMC ADC: 00
Enables DC-In VSense divider when AC present.
2.2KHz

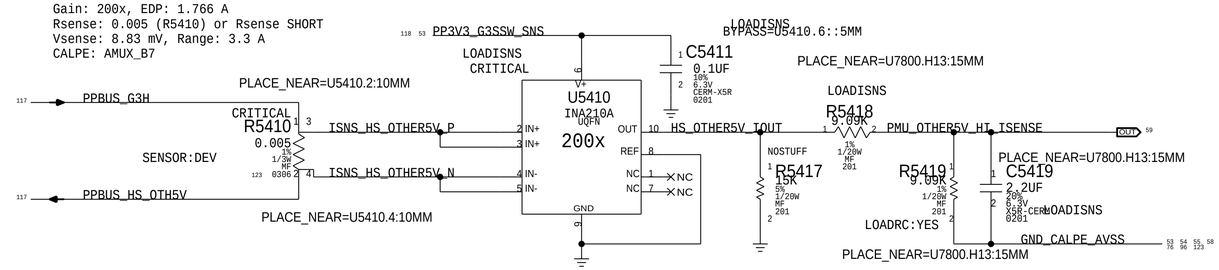


J152 Sensor Settings

IC	Vref	Vmax	SMC Sample Freq.	ADR RC filter
H9M	1.25	1.8	10kHz	0.1ms
CALPE	1.5	5.0	100Hz	10ms
EADC	2.5	5.0	1-2Hz (10Hz)	100ms

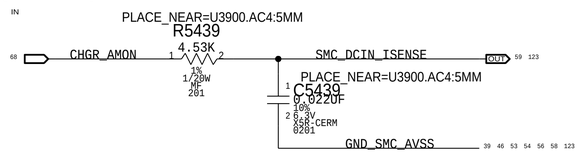
OTHER 5V High Side Current Sense (IO5R)

Gain: 200x, EDP: 1.766 A
Rsense: 0.005 (R5410) or Rsense SHORT
Vsense: 8.83 mV, Range: 3.3 A
CALPE: AMUX_B7



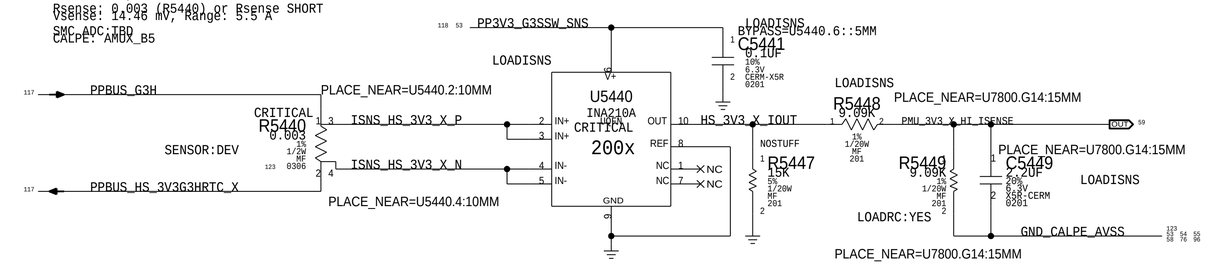
DC-IN Current Sense (ID0R)

DISCharger Gain: 20x, EDP: 4.6 A
Rsense: 0.010 (R7020)
SMC ADC: 01



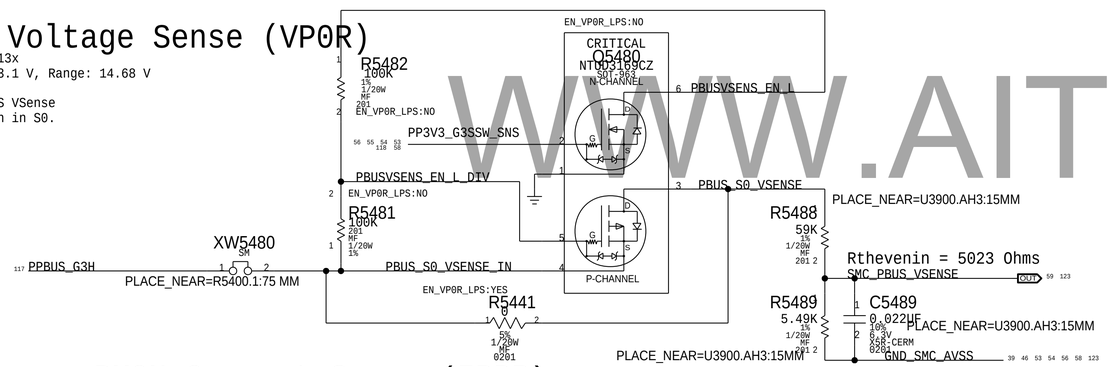
LEFT SIDE 3.3V High Side Current Sense (IOLR)

Gain: 200x, EDP: 4.82 A
Rsense: 0.003 (R5440) or Rsense SHORT
Vsense: 14.46 mV, Range: 5.5 A
SMC ADC:TBD
CALPE: AMUX_B5



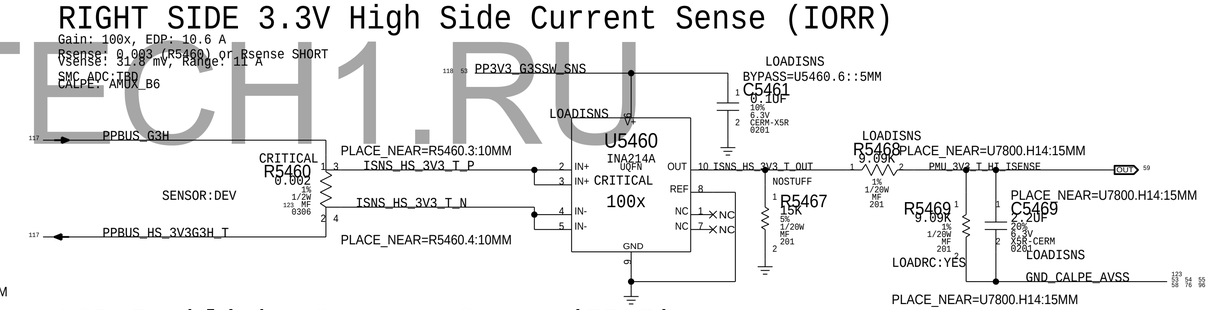
PBUS Voltage Sense (VP0R)

Gain: 0.08513x
Vnominal: 13.1 V, Range: 14.68 V
SMC ADC: 02
Enables PBUS VSense divider when in S0.



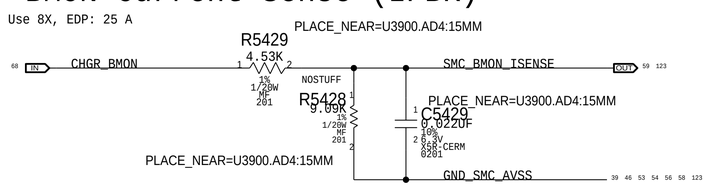
RIGHT SIDE 3.3V High Side Current Sense (IORR)

Gain: 100x, EDP: 10.6 A
Rsense: 0.003 (R5460) or Rsense SHORT
Vsense: 31.8 mV, Range: 11 A
SMC ADC:TBD
CALPE: AMUX_B6



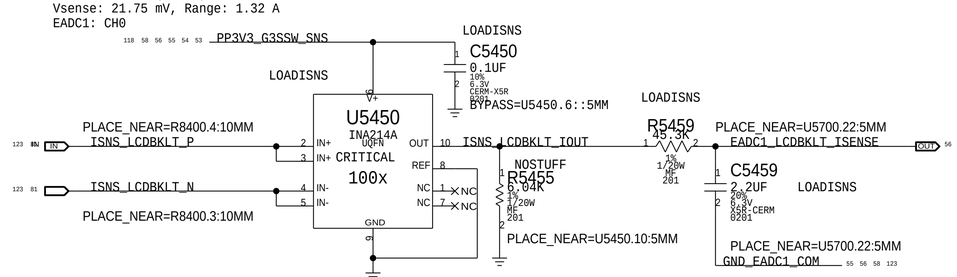
Discharger BMON Current Sense (IPBR)

Charger Gain: 8X OR 64x, Use 8X, EDP: 25 A
Rsense: 0.005 (R7060)
SMC ADC: 03



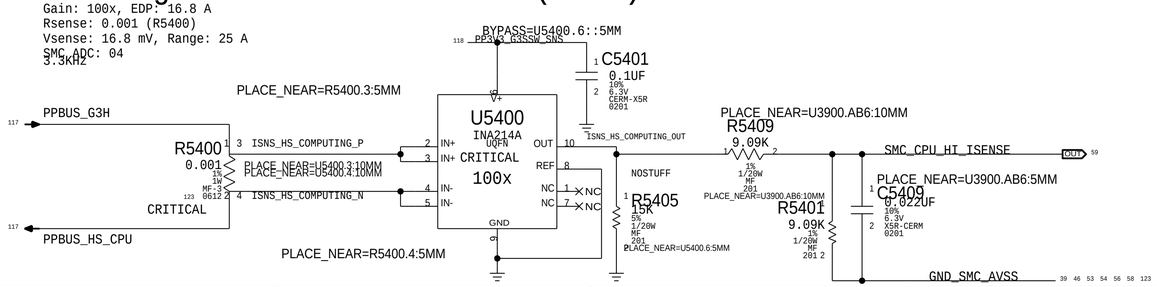
LCD Backlight Current Sense (IBLR)

Gain: 100x. EDP: 0.87 A
Rsense: 0.025 (R8400)
Vsense: 21.75 mV, Range: 1.32 A
EADC1: CH0



CPU High Side Curent Sense (IC0R)

Gain: 100x, EDP: 16.8 A
Rsense: 0.001 (R5400)
Vsense: 16.8 mV, Range: 25 A
SMC ADC: 04
3.3kHz



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R5449,R5469,R5419		LOADRC:NO

BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors High Side

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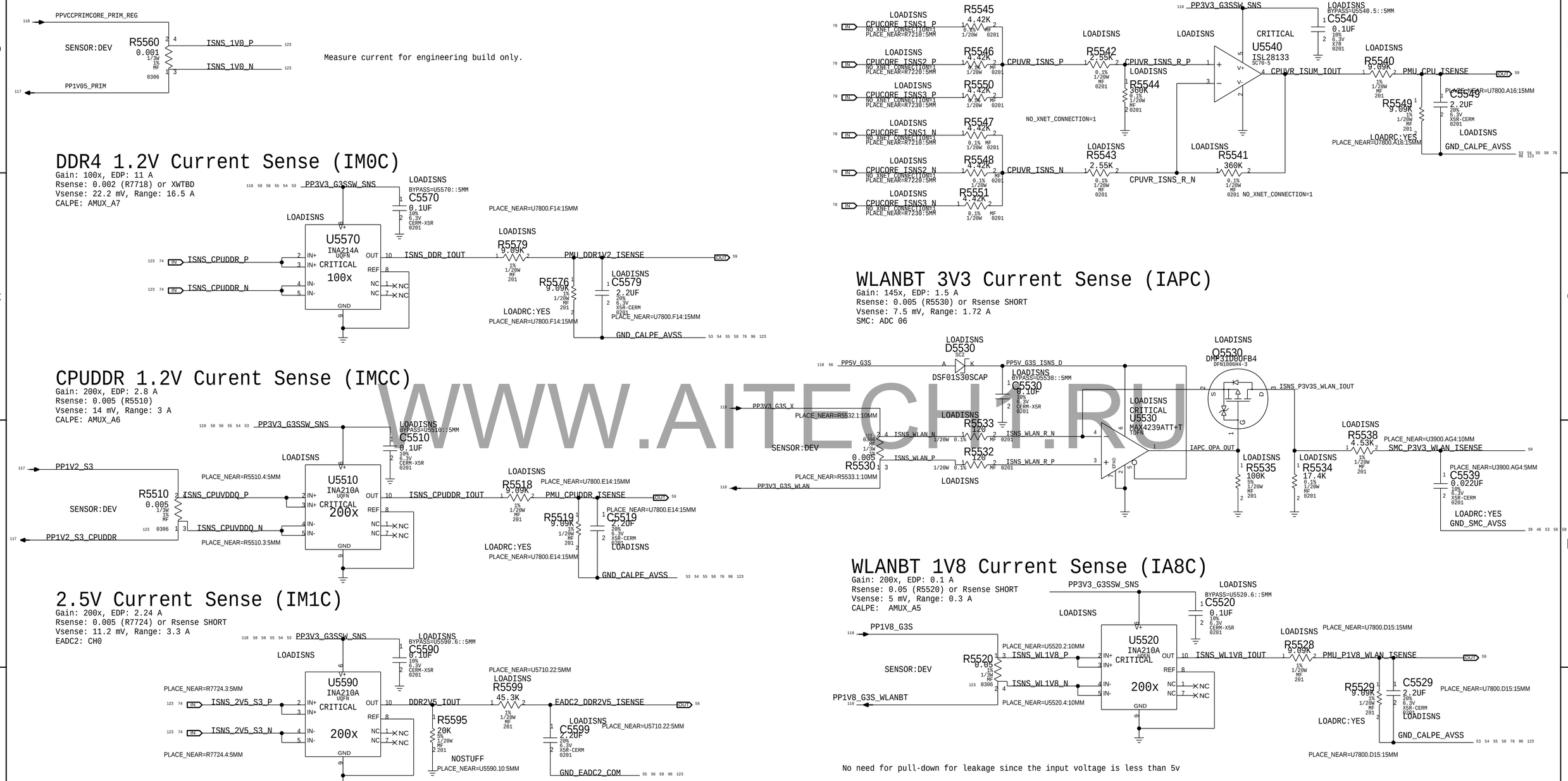

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	5	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R5576,R5519,R5549,C5539,R5529		LOADRC:NO

PAGE TITLE
Power Sensors Load Side

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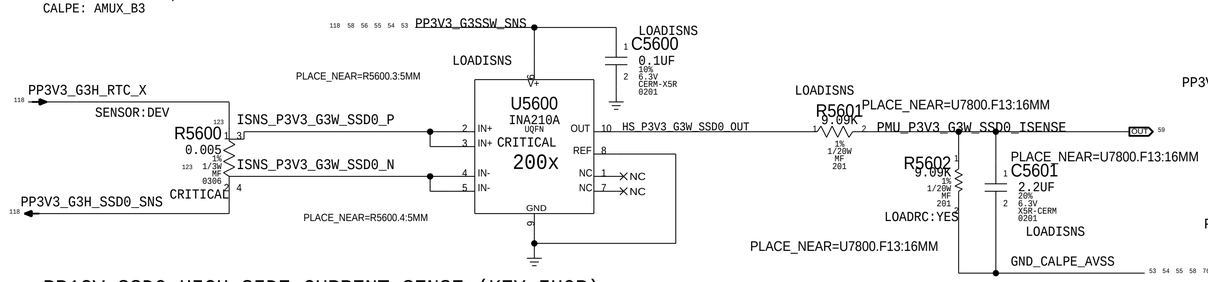
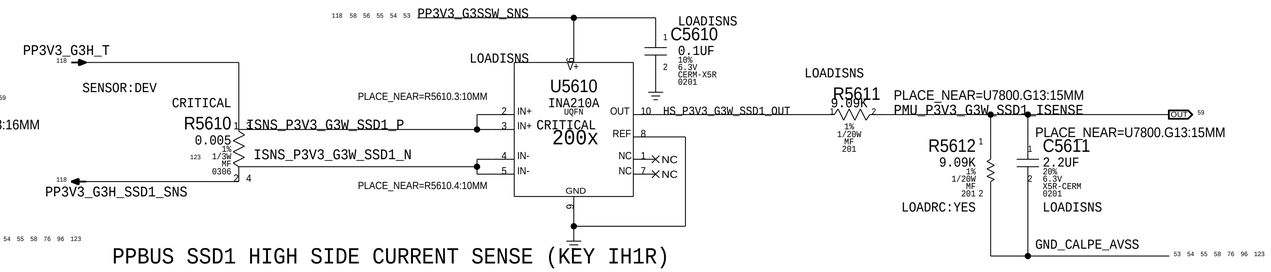
PP3V3_G3W_SSD0 HIGH SIDE CURRENT SENSE (KEY IH0C)

GAIN: 200X, EDP: 1.48 A
RSENSE: 0.005 (RK710) OR RSENSE SHORT
VSENSE: 13 MV, RANGE: 2.5 A
CALPE: AMUX_B3



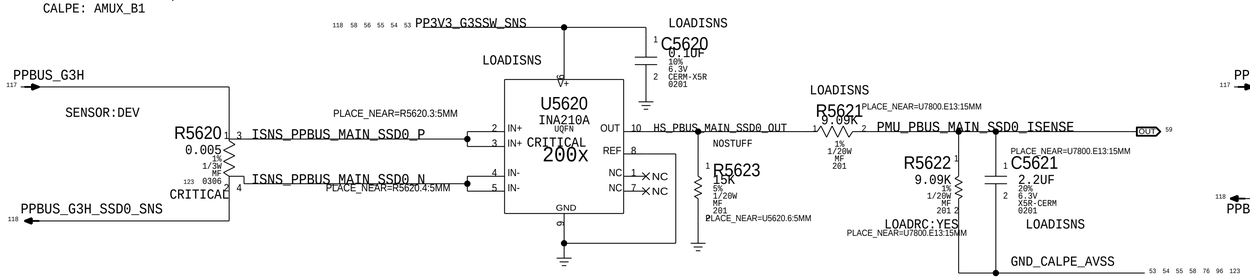
PP3V3_G3W_SSD1 HIGH SIDE CURRENT SENSE (KEY IH1C)

GAIN: 200X, EDP: 1.48 A
RSENSE: 0.005 (RK760) OR RSENSE SHORT
VSENSE: 13 MV, RANGE: 2.5 A
CALPE: AMUX_B4



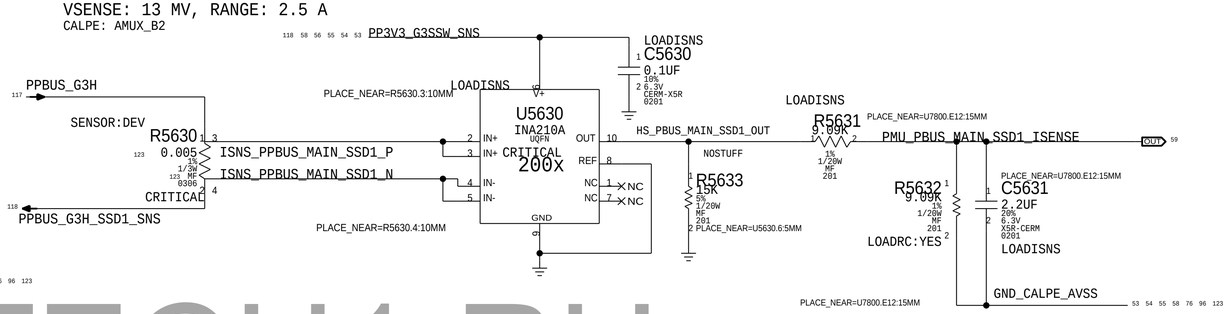
PP12V SSD0 HIGH SIDE CURRENT SENSE (KEY IH0R)

GAIN: 200X, EDP: 0.5 A
RSENSE: 0.005 (RK610) OR RSENSE SHORT
VSENSE: 13 MV, RANGE: 2.5 A
CALPE: AMUX_B1



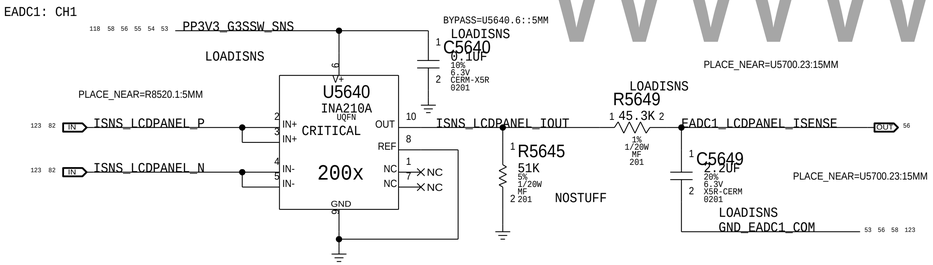
PPBUS SSD1 HIGH SIDE CURRENT SENSE (KEY IH1R)

GAIN: 200X, EDP: 0.5 A
RSENSE: 0.005 (R5607) OR RSENSE SHORT
VSENSE: 13 MV, RANGE: 2.5 A
CALPE: AMUX_B2



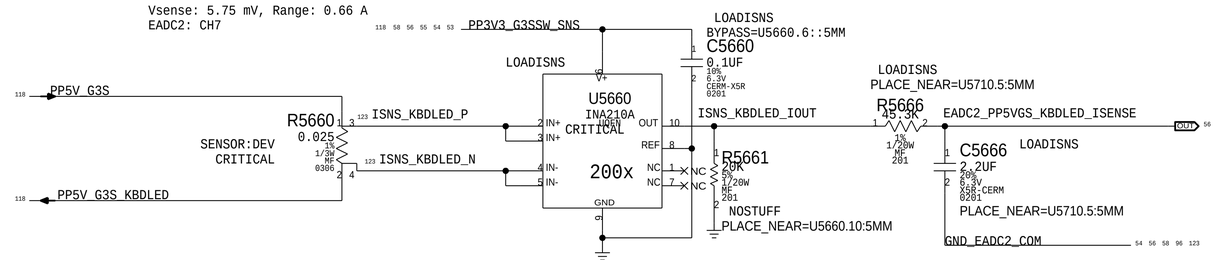
LCD Panel Current Sense (ILDC)

Gain: 200x. EDP: 1 A
RSENSE: 0.01 (R8520) or Rsense SHORT
Vsense: 5 mV, Range: 1.25 A
EADC1: CH1



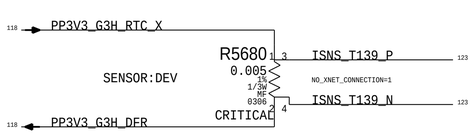
Keyboard backlight Current Sense (IKBC)

Gain: 200x, EDP: 0.23 A
Rsense: 0.025 (R5660) or Rsense SHORT
Vsense: 5.75 mV, Range: 0.66 A
EADC2: CH7



T139 Current Sense resistor

EDP: 0.06 A
Rsense: 0.05 (R5680) or Rsense SHORT



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	4	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R5602,R5612,R5622,R5632		LOADRC:NO

BOM_COST_GROUP=SENSORS

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PAGE TITLE: Power Sensors Extended 1

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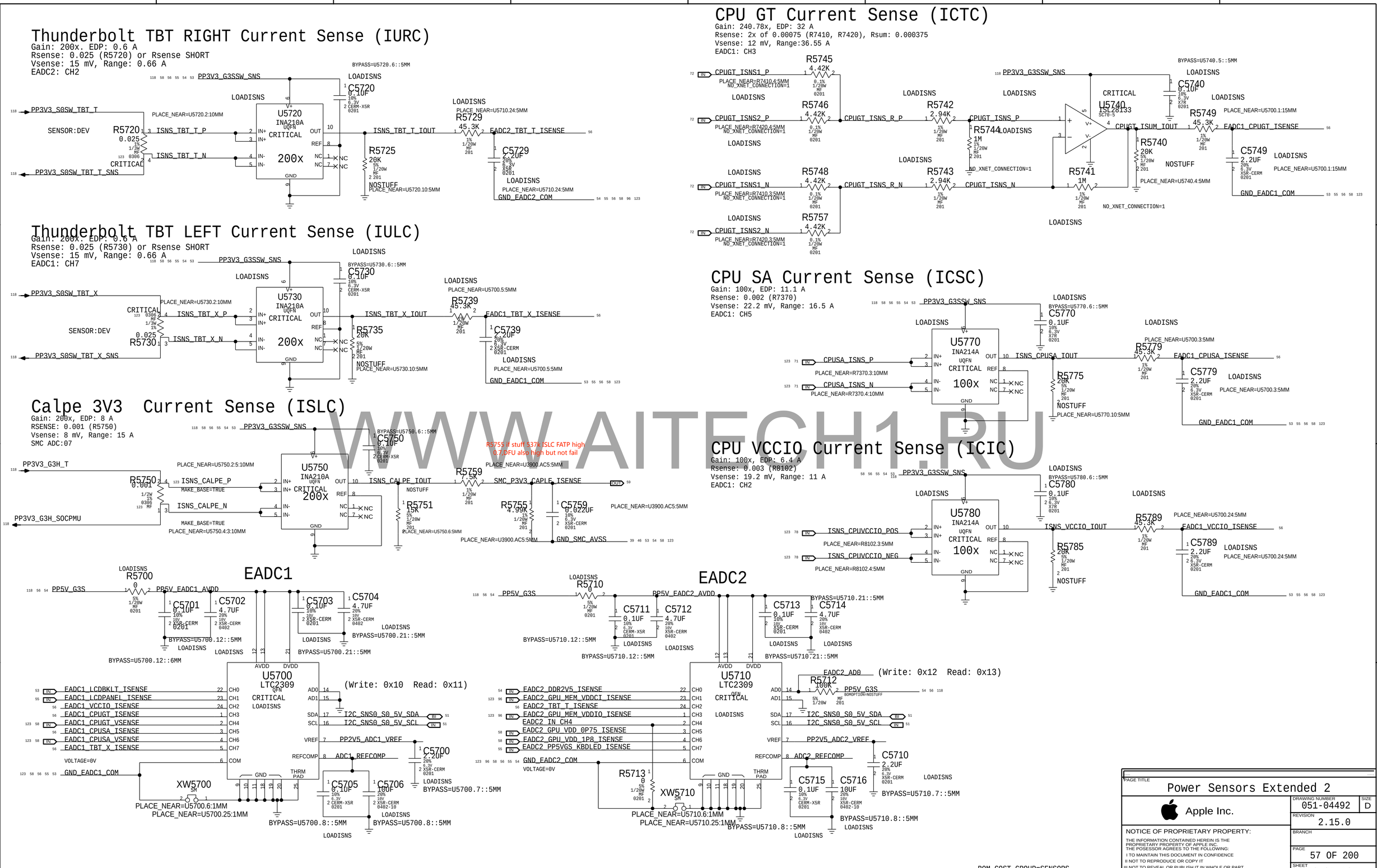

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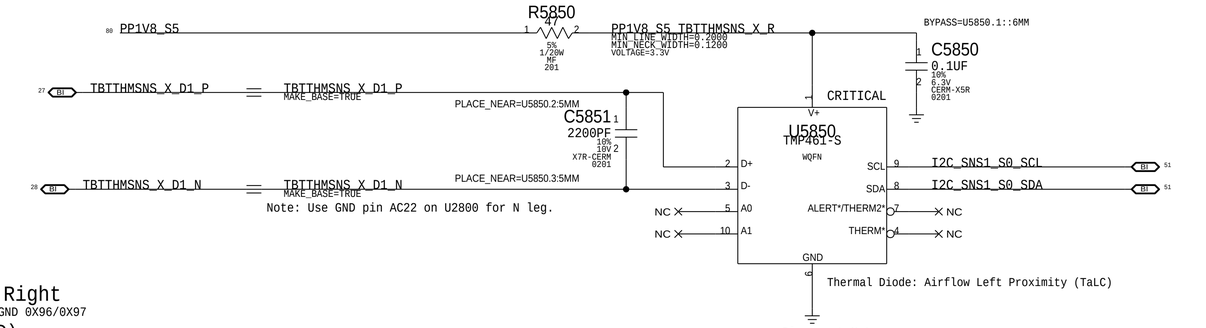
Thermal Sensor A:

Thunderbolt Die, Airflow Left

U5850 I2C Address:TMP461 A1->Floating A0->Floating 0X98/0X99

Thermal Diode: TBT Die (TTLD)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.



Note: Use GND pin AC22 on U2800 for N leg.

Thermal Diode: Airflow Left Proximity (TaLC)

Placement Note:
Place U5850 on the TOP side, on the left portion of the board, 1" to the right of USB connector.

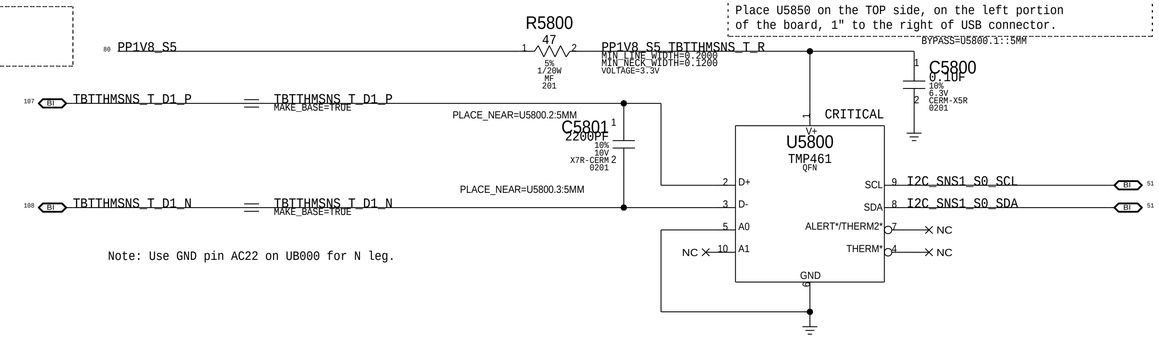
Thermal Sensor C:

Thunderbolt Die, Air Flow Right

U5800 I2C Address:TMP461 A1->Floating A0->GND 0X96/0X97

Thermal Diode: TBT Die (TTRD)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.



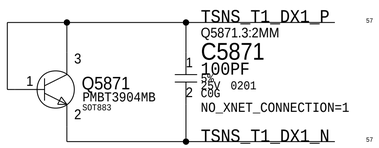
Note: Use GND pin AC22 on UB000 for N leg.

Thermal Diode: Airflow Right Proximity (TaRC)

Placement Note:
Place U5800 on the TOP side, on the left portion of the board, 1" to the right of USB connector.

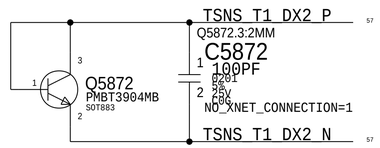
THERMAL DIODE: CPU PROX (KEY TC0P)

Placement Note:
Place Q5871 under the CPU ON BOTTOM SIDE



THERMAL DIODE: FIN STACK LEFT (KEY TH2H)

Placement Note:
Place Q5872,AIRFLOW THERMAL INDICATOR,ABOVETHE X100, ON THE TOP SIDE



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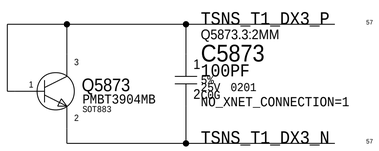
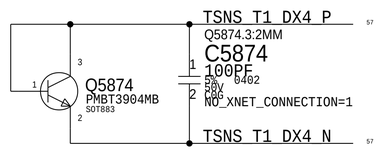
THERMAL DIODE: FIN STACK RIGHT (KEY TH1H)

Placement Note:
Place Q5873 AT THE CORNER NEAR RIGHT FAN, ON THE TOP SIDE



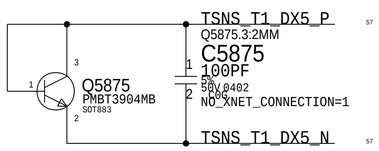
THERMAL DIODE: Memory Proximity (KEY TM0P)

Place Q5874 between two rows of Memory devices, between channel A and CHANNEHL b PN BOTTOM SIDES



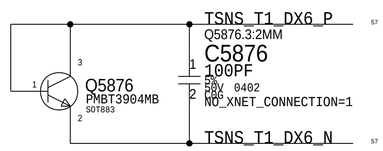
THERMAL DIODE: X100 PROXIMITY (KEY TW0P)

Place Q5875 near X100 on bottom



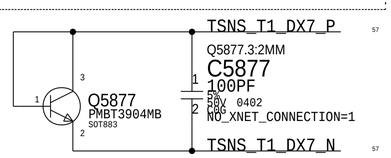
THERMAL DIODE: GPU PROXIMITY(TG0P)

Place Q5876 near GPU, Top side, Opposite side of GPU



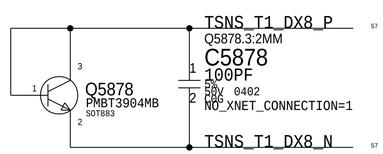
THERMAL DIODE: GPU VR PROXIMITY(TG1P)

Place Q5877 near GPU VR, Bottom side

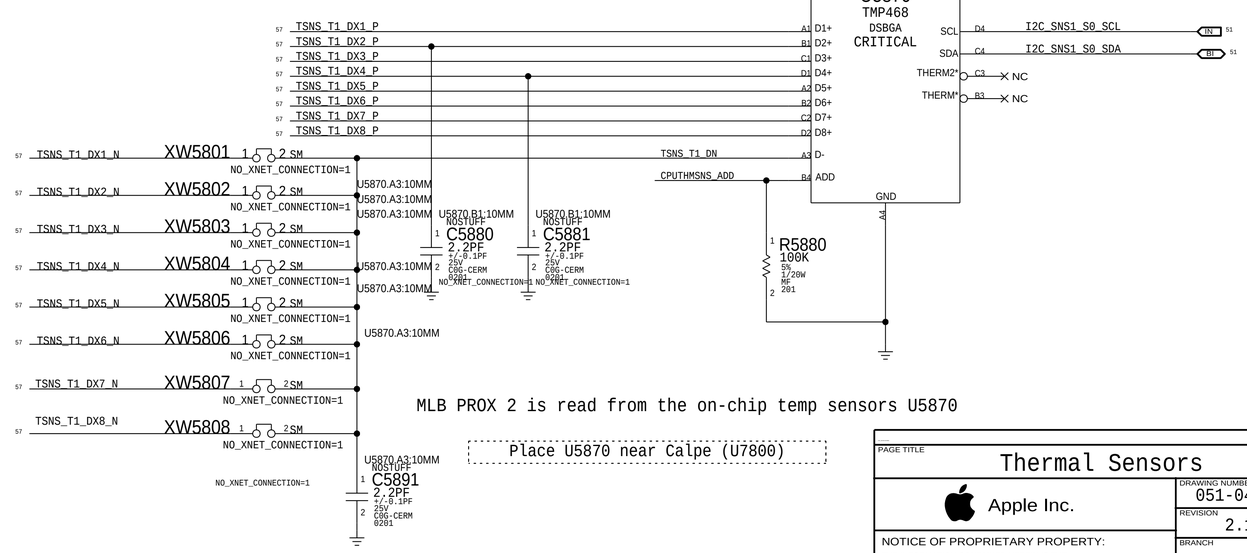


THERMAL DIODE: GPU VRAM PROXIMITY(TGVP)

Place Q5878 near GPU VRAM.



MLB THERMAL SENSE 1 (TMP468)
I2C DEVICE ADDRESS 0X48:
I2C WRITE 0X90, I2C READ 0X91



MLB PROX 2 is read from the on-chip temp sensors U5870

Place U5870 near Calpe (U7800)

BOM_COST_GROUP=SENSORS

PAGE TITLE	Thermal Sensors
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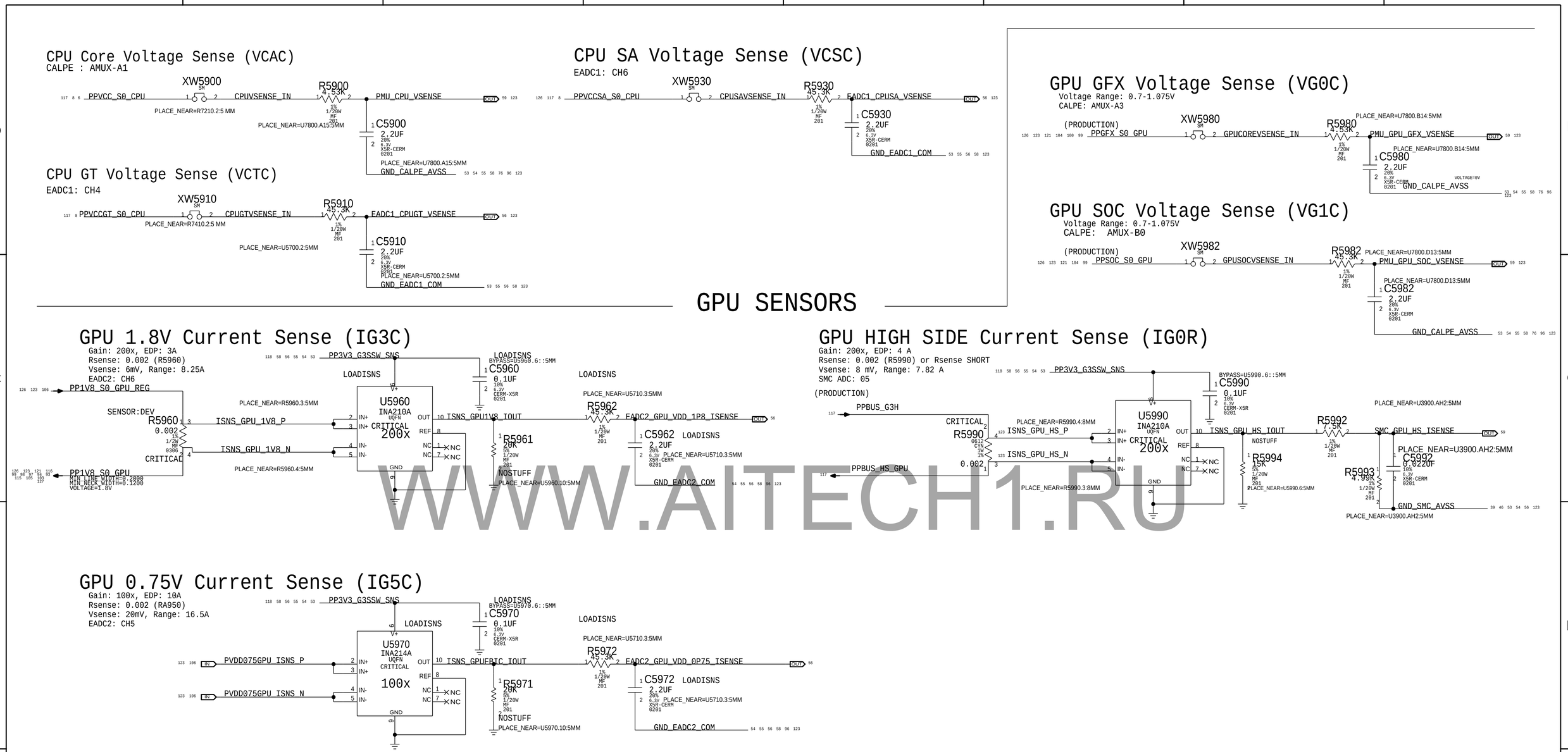

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Power Sensor Extended 3

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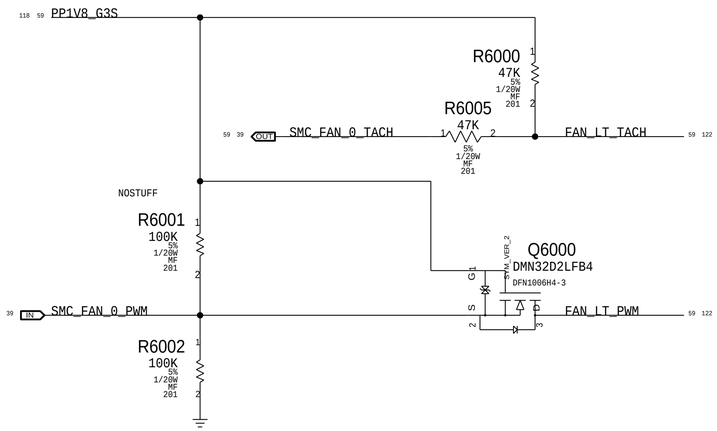
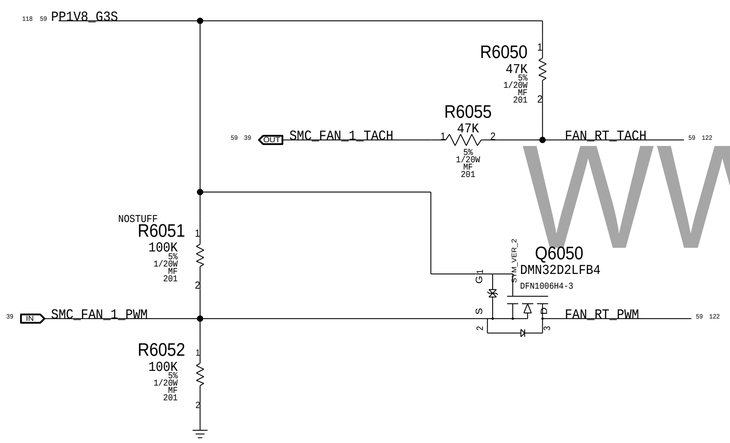
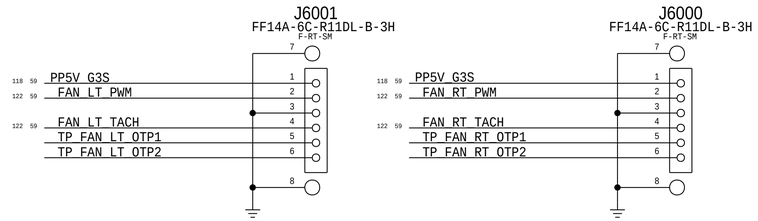
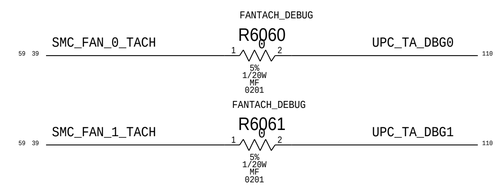
FAN CONNECTOR

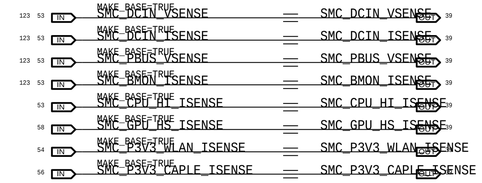




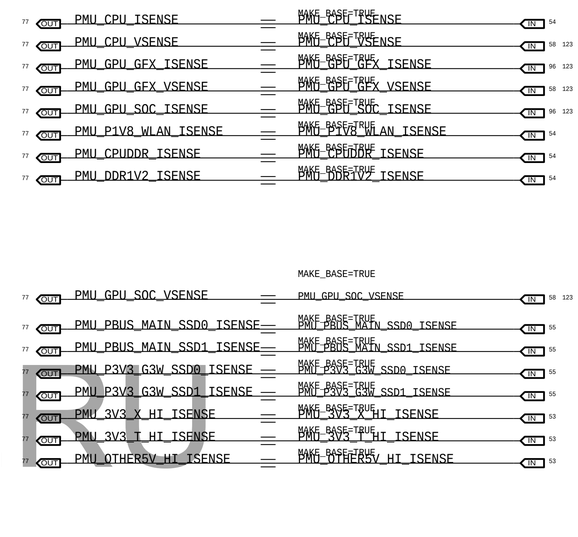




H9M SMC ADC Assignments



CALPE AMUX Assignments



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BOM_COST_GROUP=FAN

PAGE TITLE
Fans/SMC/AMUX Support

Apple Inc.

DRAWING NUMBER 051-04492 SIZE D
REVISION 2.15.0
BRANCH
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BOM_COST_GROUP=AUDIO

PAGE TITLE	Audio Placeholder
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	REVISION 2.15.0
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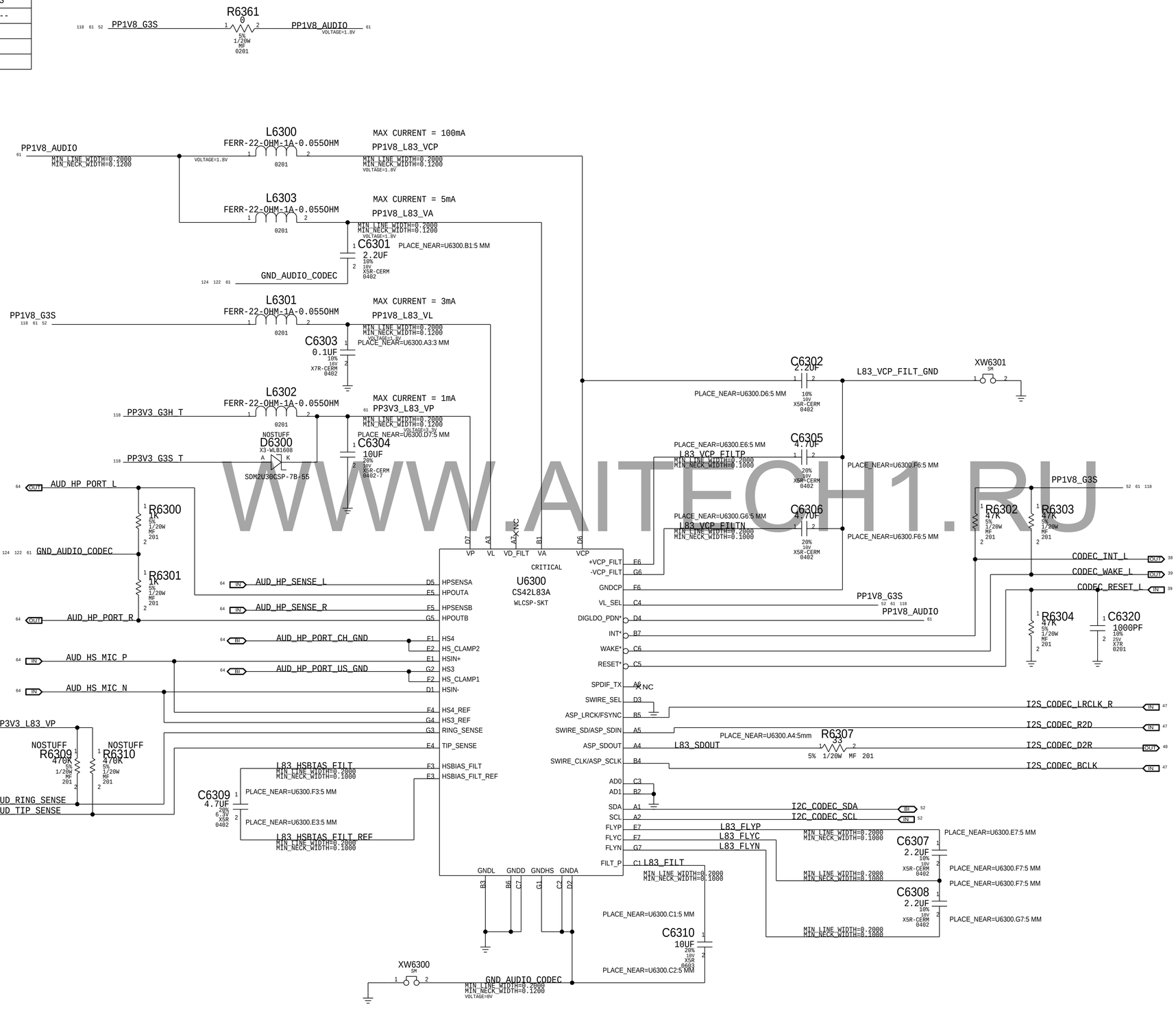
AUDIO JACK CODEC I2C ADDRESS		
AD1	AD0	ADDRESS
GND	GND	0x48 <--
GND	1.8V	0x49
1.8V	GND	0x4A
1.8V	1.8V	0x4B



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DESIGN: X502/DEV_MLB_U
LAST CHANGE: Wed Feb 18 17:31:01 2015

PAGE TITLE
Audio Jack Codec

Apple Inc.

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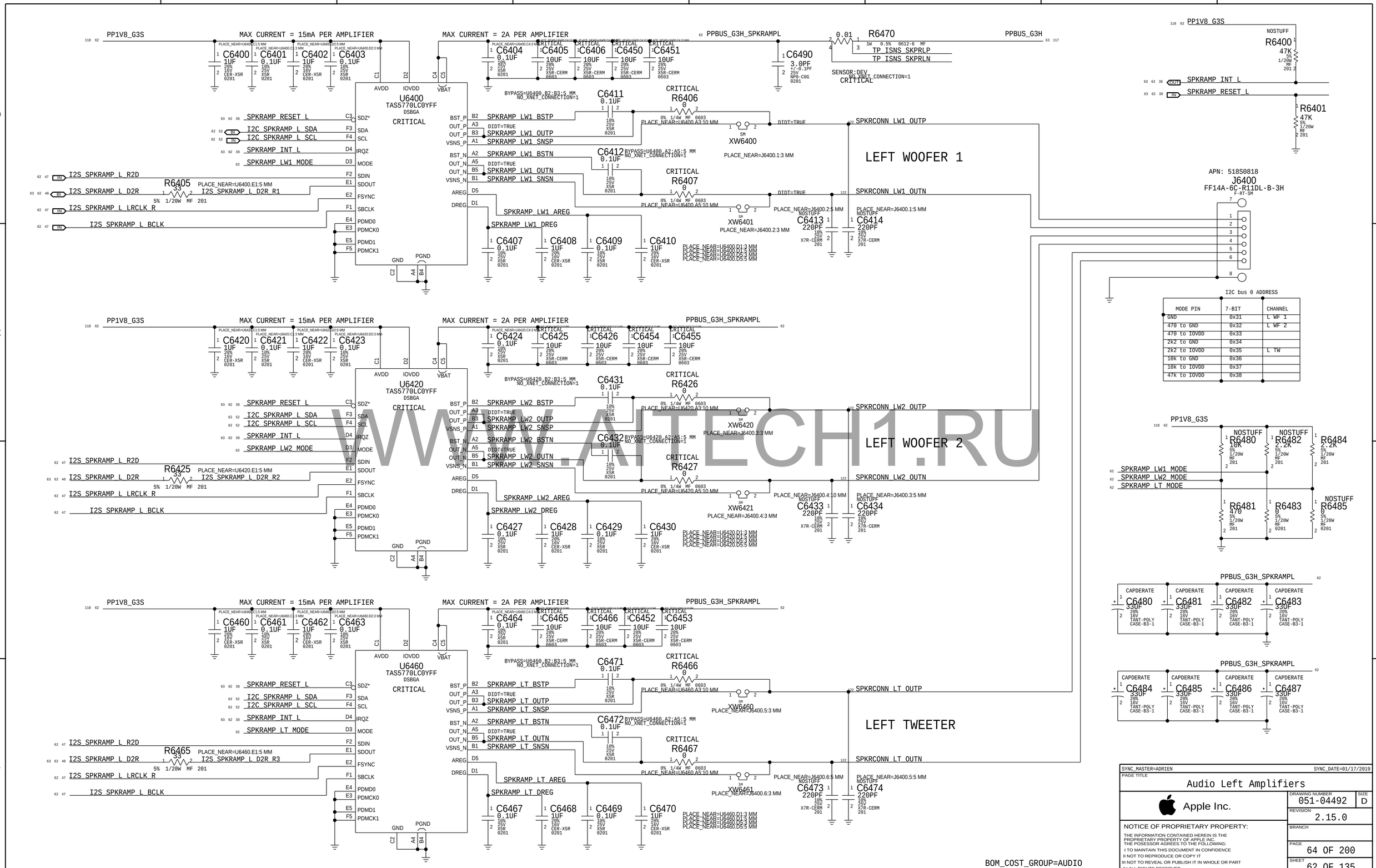

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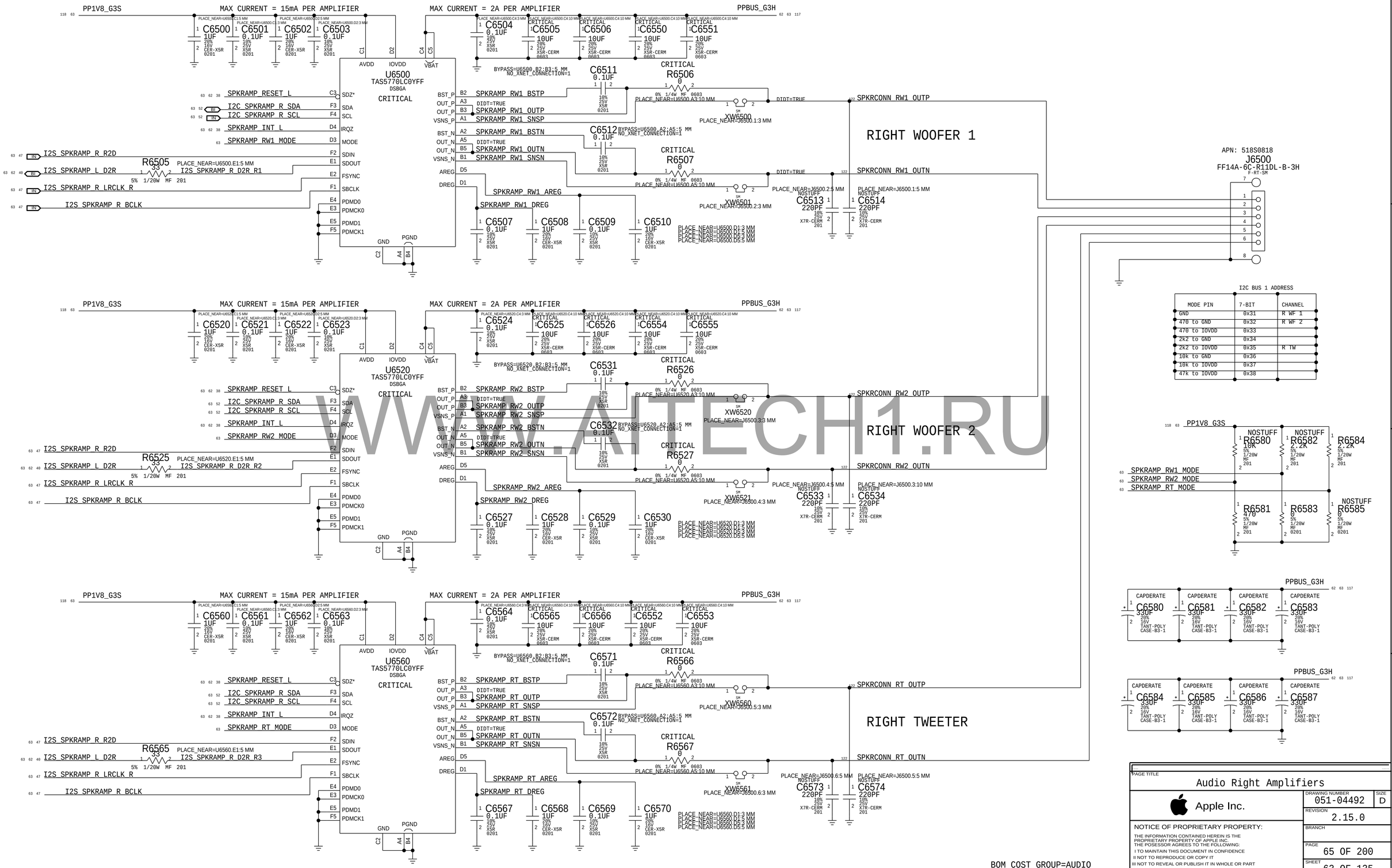

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PAGE TITLE: Audio Right Amplifiers

Apple Inc.

DRAWING NUMBER: 051-04492 | SIZE: D

REVISION: 2.15.0

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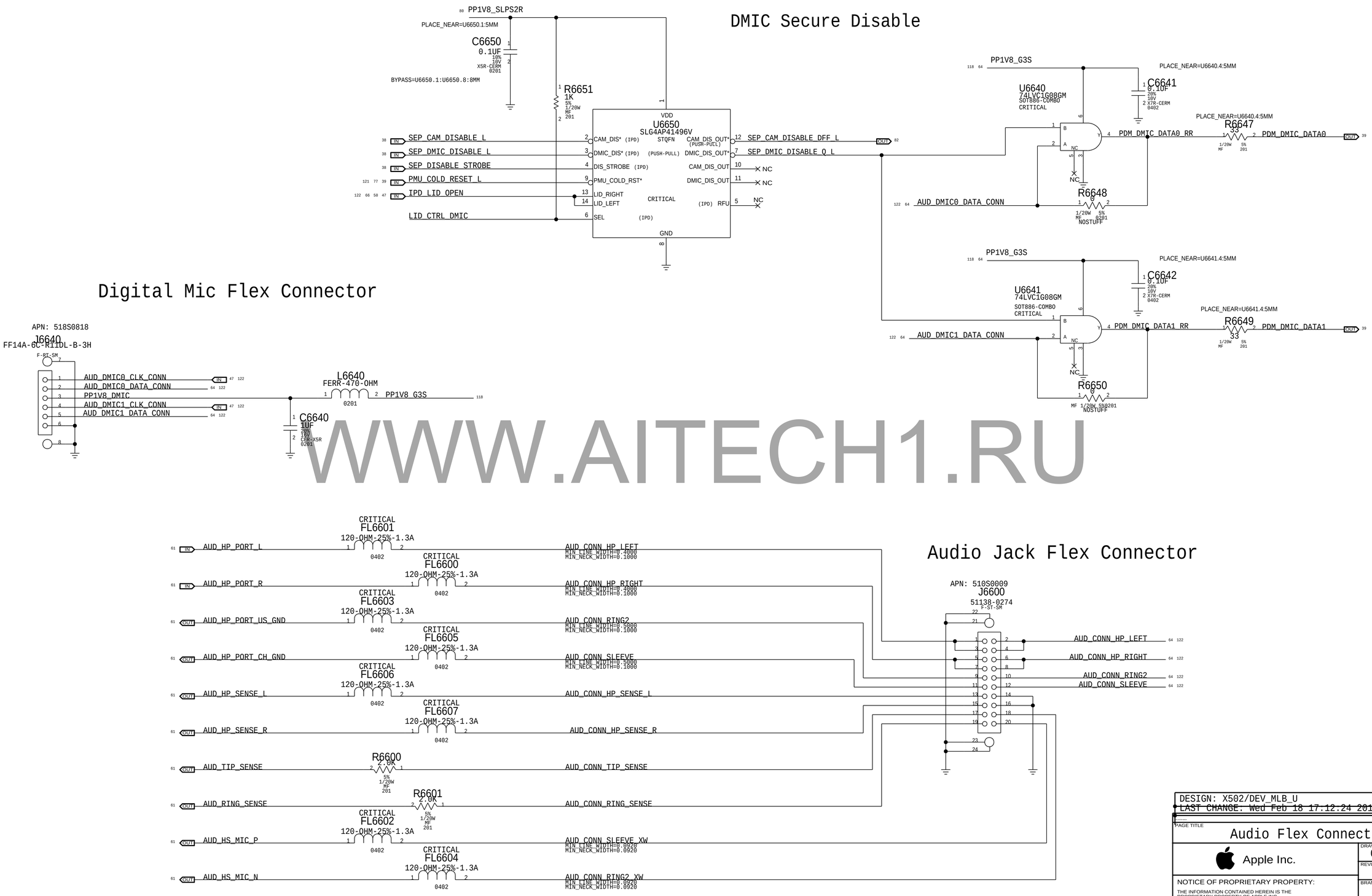
DMIC Secure Disable
PP1V8_SLPS2R
PLACE_NEAR=U6650.1:5MM
C6650
0.1UF
BYPASS=U6650.1:U6650.8:8MM
R6651
1K
U6650
SL64AP41496V
STQFN
VDD
GND
CRITICAL
SEP_CAM_DISABLE_L
SEP_DMIC_DISABLE_L
SEP_DISABLE_STROBE
PMU_COLD_RESET_L
IPD_LID_OPEN
LID_CTRL_DMIC
CAM_DIS* (IPD)
DMIC_DIS* (IPD)
DIS_STROBE (IPD)
PMU_COLD_RESET*
LID_RIGHT
LID_LEFT
SEL (IPD)
CAM_DIS_OUT* (PUSH-PULL)
DMIC_DIS_OUT* (PUSH-PULL)
CAM_DIS_OUT
DMIC_DIS_OUT
RFU (IPD)
SEP_CAM_DISABLE_DFF_L
SEP_DMIC_DISABLE_Q_L
NC
PP1V8_G3S
PLACE_NEAR=U6640.4:5MM
U6640
74LVC1G08GM
SOT886-COMBO
CRITICAL
C6641
0.1UF
PLACE_NEAR=U6640.4:5MM
R6647
33
PDM_DMIC_DATA0_RR
PDM_DMIC_DATA0
R6648
0
NOSTUFF
AUD_DMIC0_DATA_CONN
PP1V8_G3S
PLACE_NEAR=U6641.4:5MM
U6641
74LVC1G08GM
SOT886-COMBO
CRITICAL
C6642
0.1UF
PLACE_NEAR=U6641.4:5MM
R6649
33
PDM_DMIC_DATA1_RR
PDM_DMIC_DATA1
R6650
0
NOSTUFF
AUD_DMIC1_DATA_CONN
Digital Mic Flex Connector
APN: 518S0818
J6640
FF14A-6C-R11DL-B-3H
F-RT-SM
AUD_DMIC0_CLK_CONN
AUD_DMIC0_DATA_CONN
PP1V8_DMIC
AUD_DMIC1_CLK_CONN
AUD_DMIC1_DATA_CONN
L6640
FERR-470-OHM
0201
PP1V8_G3S
C6640
10UF
CER-X5R
0201
WWW.AITECH1.RU
Audio Jack Flex Connector
APN: 510S0009
J6600
51138-0274
F-ST-SM
AUD_HP_PORT_L
AUD_HP_PORT_R
AUD_HP_PORT_US_GND
AUD_HP_PORT_CH_GND
AUD_HP_SENSE_L
AUD_HP_SENSE_R
AUD_TIP_SENSE
AUD_RING_SENSE
AUD_HS_MIC_P
AUD_HS_MIC_N
FL6601
FL6600
FL6603
FL6605
FL6606
FL6607
FL6602
FL6604
120-OHM-25%-1.3A
0402
CRITICAL
R6600
2.0K
R6601
2.0K
AUD_CONN_HP_LEFT
AUD_CONN_HP_RIGHT
AUD_CONN_RING2
AUD_CONN_SLEEVE
AUD_CONN_HP_SENSE_L
AUD_CONN_HP_SENSE_R
AUD_CONN_TIP_SENSE
AUD_CONN_RING_SENSE
AUD_CONN_SLEEVE_XW
AUD_CONN_RING2_XW
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MIN_NECK_WIDTH=0.0920
BOM_COST_GROUP=AUDIO
DESIGN: X502/DEV_MLB_U
LAST CHANGE: Wed Feb 18 17:12:24 2015
PAGE TITLE
Audio Flex Connectors
Apple Inc.
DRAWING NUMBER
051-04492
SIZE
D
REVISION
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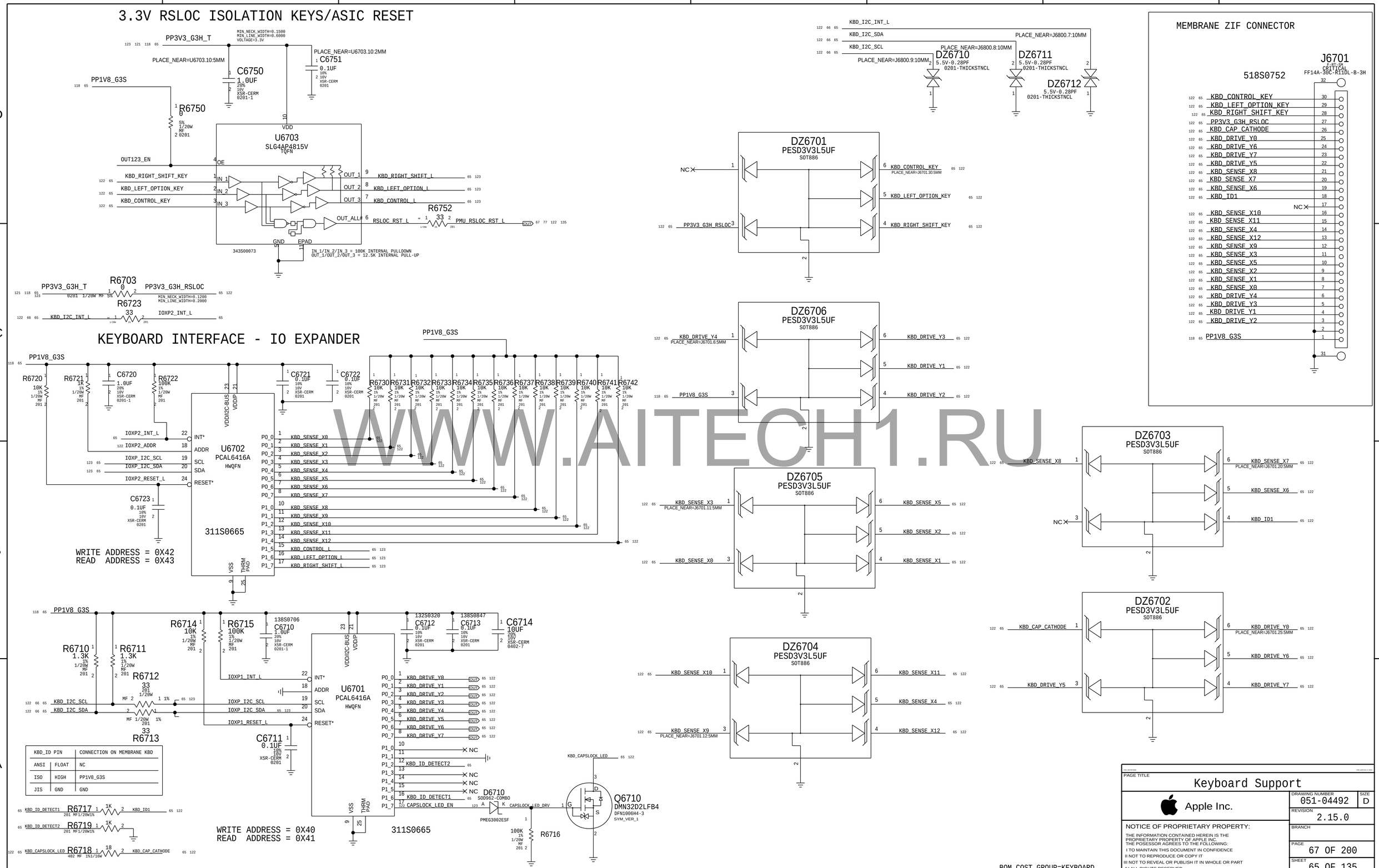

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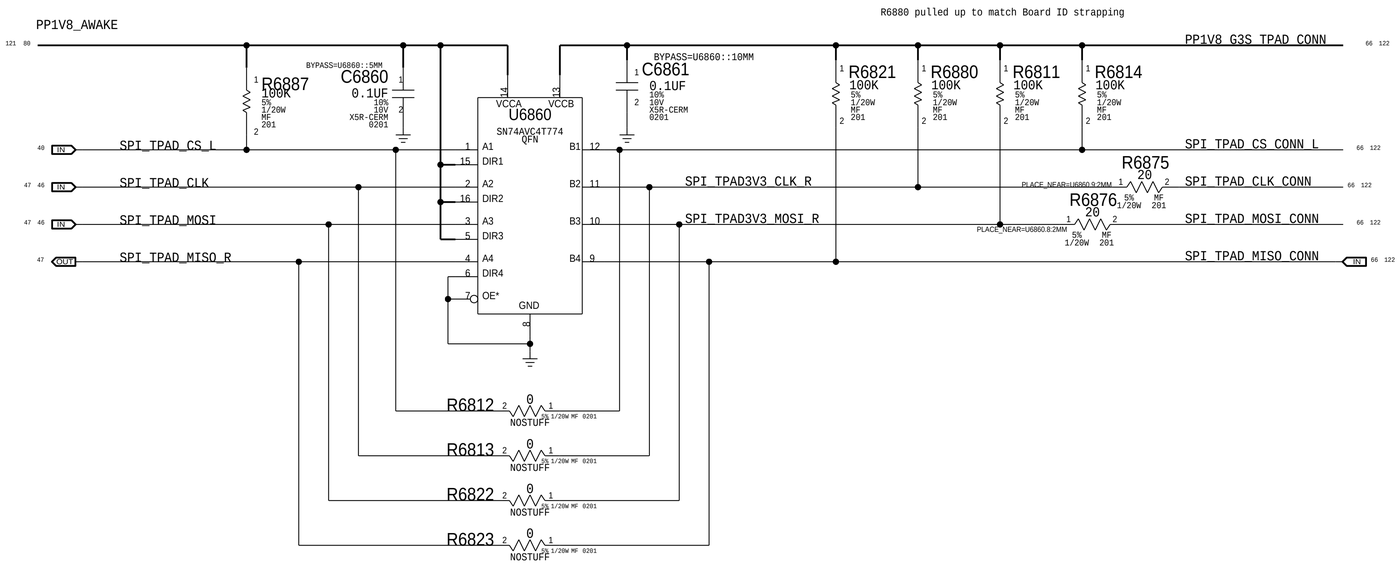
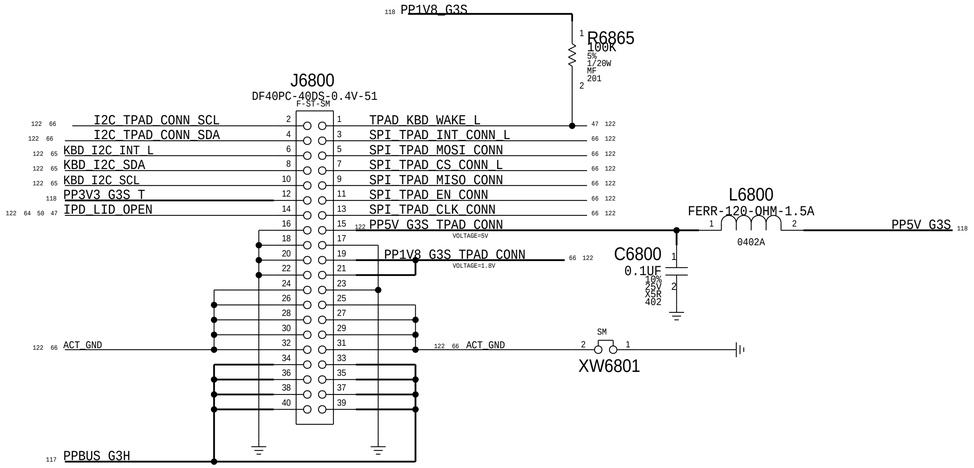
TPAD SPI AWAKE , G3S POWER RAILS ISOLATION, PULL-UPS ON G3S SIDE NEED TO MATCH BOARD_ID



TPAD CONNECTOR



516S00177, MATE WITH 516S00054

TPAD I2C, INT

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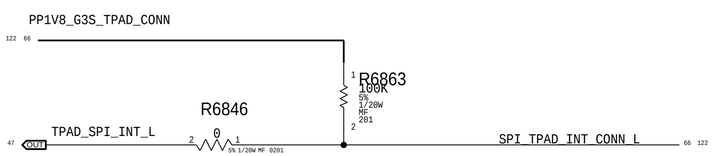
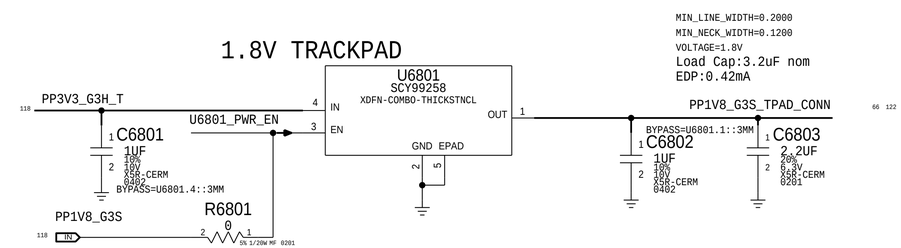
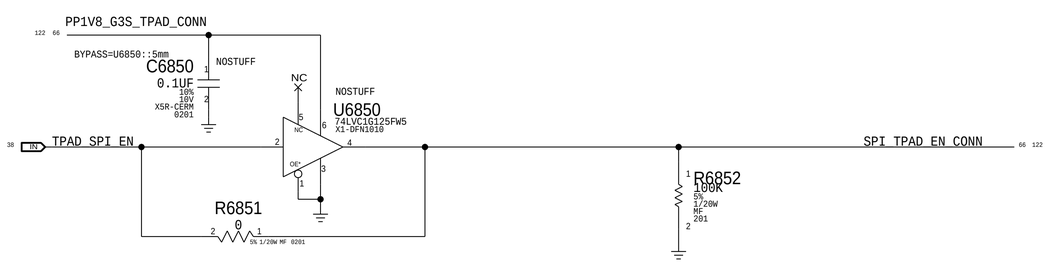


1.8V TRACKPAD



(Placeholder for 450mA part symbol)

TPAD SPI_EN G3S POWER DOMAIN



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SYNC_MASTER=RAYMOND	SYNC_DATE=01/17/2019
PAGE TITLE	Trackpad Support
Apple Inc.	DRAWING NUMBER 051-04492 / SIZE D
	REVISION 2.15.0
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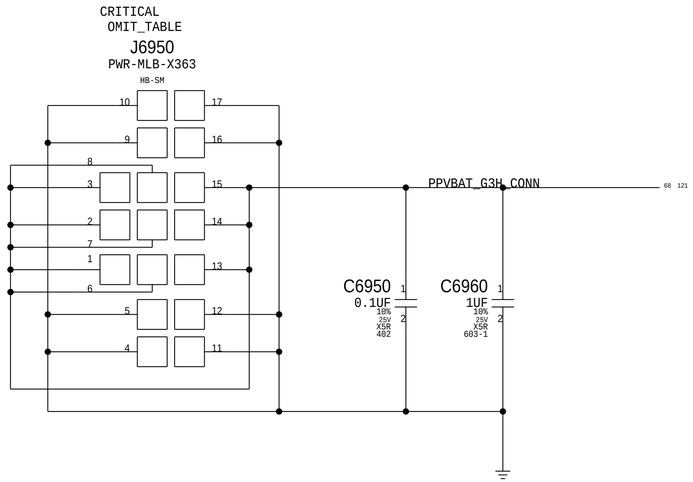
	PAGE 68 OF 200
	SHEET 66 OF 135

J80 Battery Hotbar Flex Pads 998-03902
Flex Pad TO MLB 998-03780.



BMU POWER FLEX HOTBAR'd TO THE MLB:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
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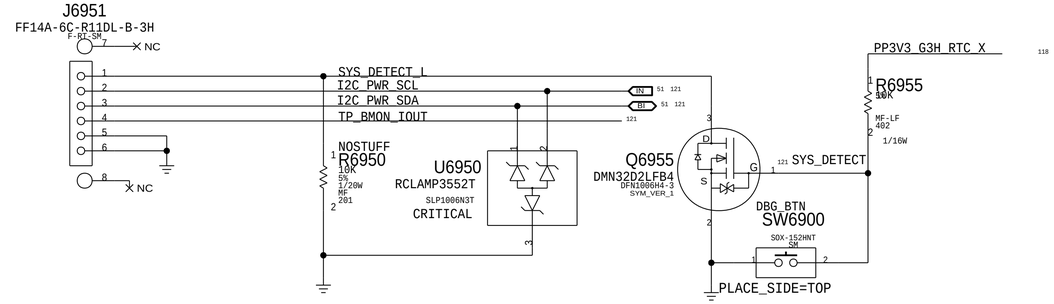
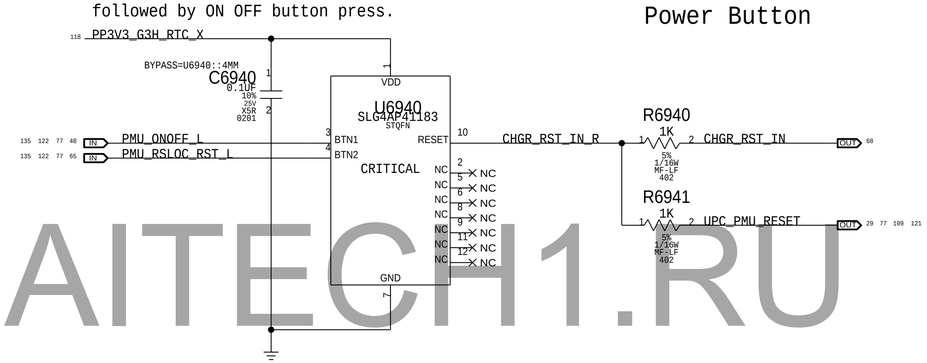
APN:518S0818



SMC Reset Circuit

Right Shift & Left Option Control
followed by ON OFF button press.



Power Button

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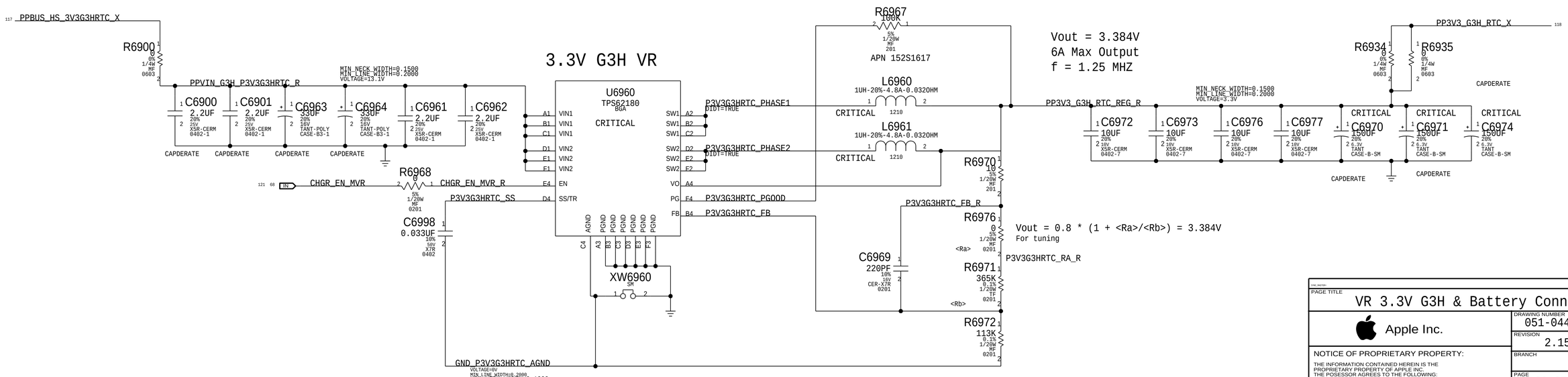

PAGE TITLE	VR 3.3V G3H & Battery Conn
Apple Inc.	DRAWING NUMBER 051-04492 · SIZE D
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NOTICE OF PROPRIETARY PROPERTY:	BRANCH
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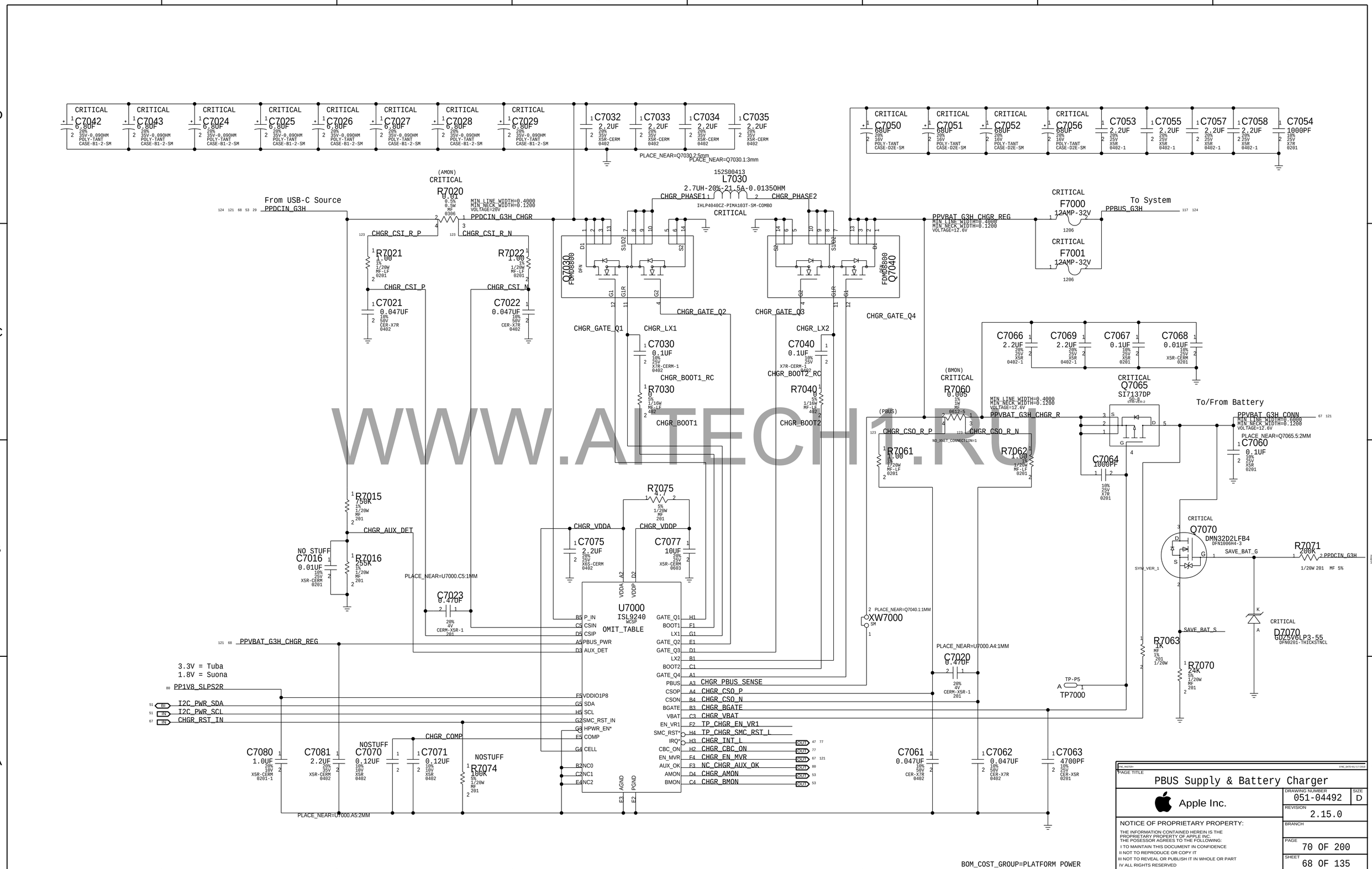
	SHEET 67 OF 135



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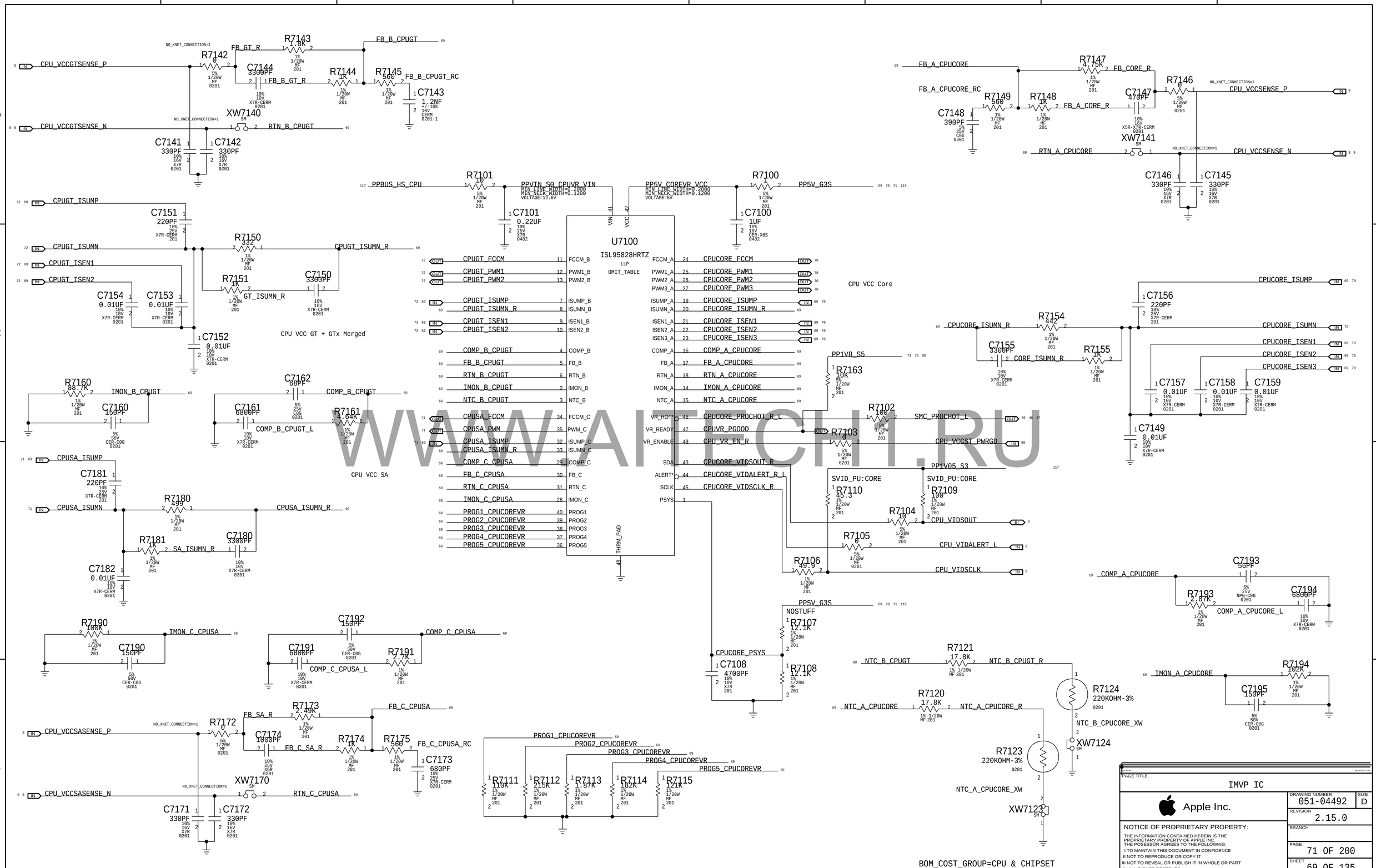

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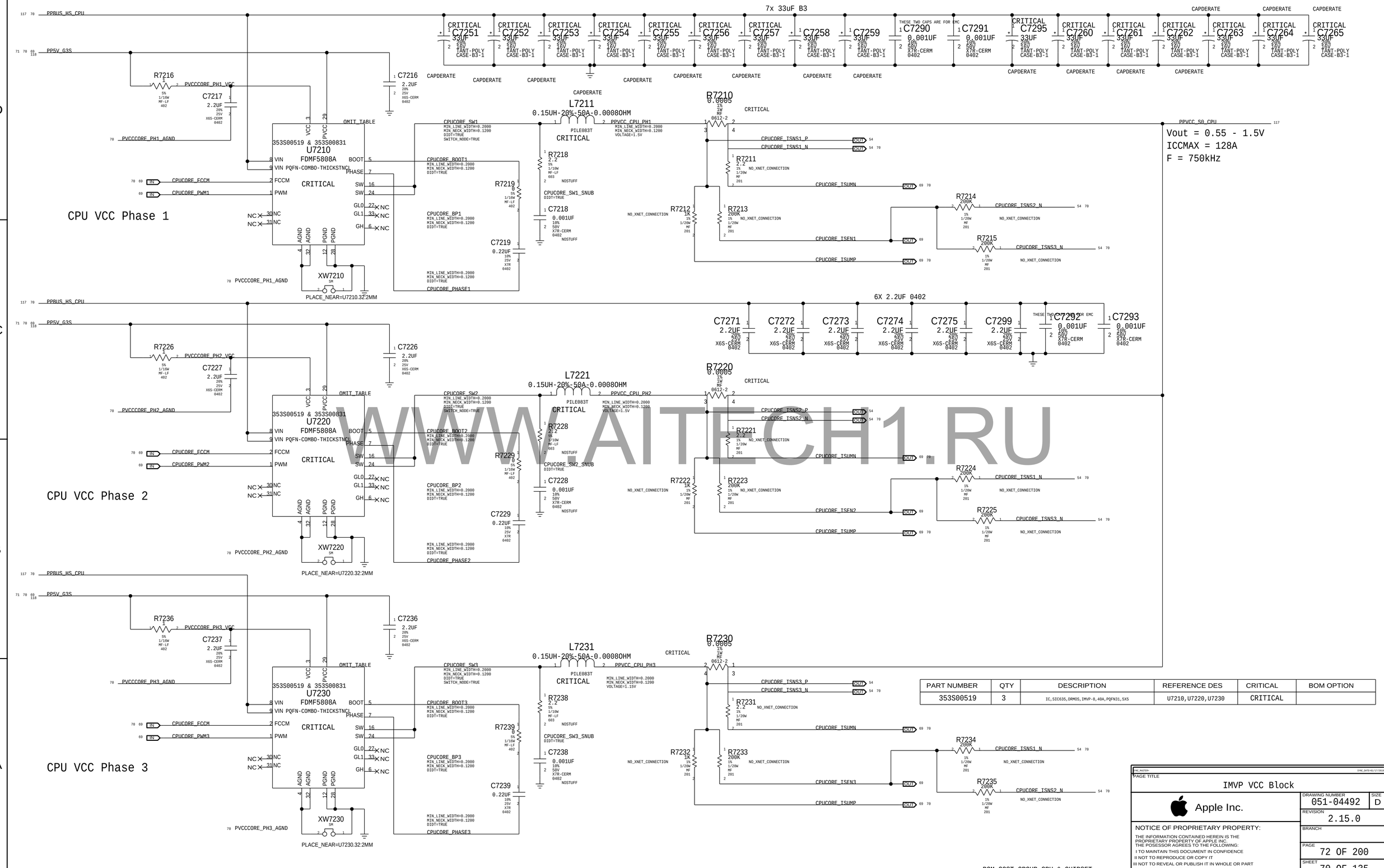

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
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PAGE TITLE

IMVP VCC Block

Apple Inc.

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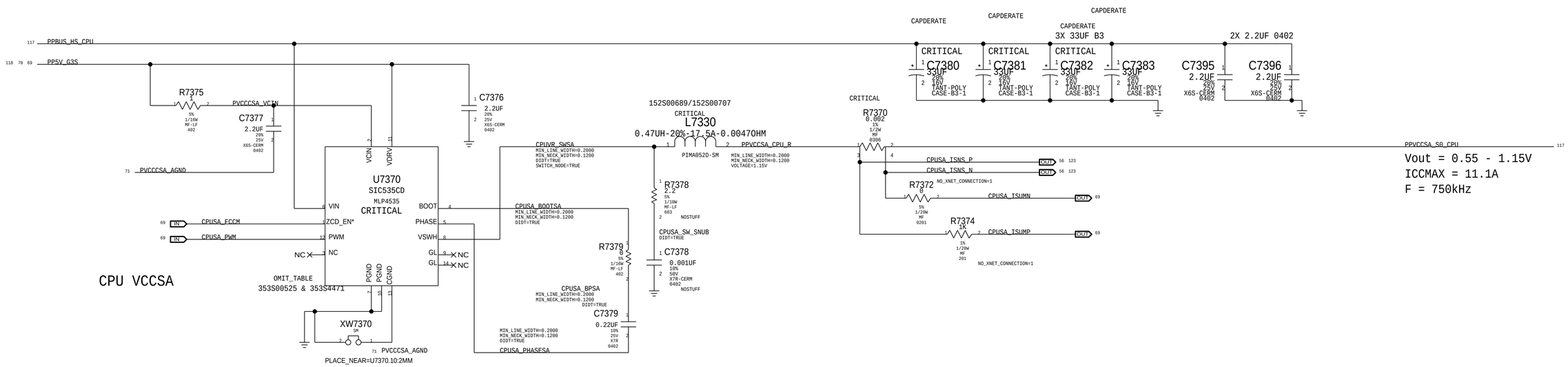

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00525	1	IC,SIC635,DRMOS,IMVP-8,40A,PQFN31,5X5	U7370	CRITICAL	

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BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
IMVP SA Block

Apple Inc.

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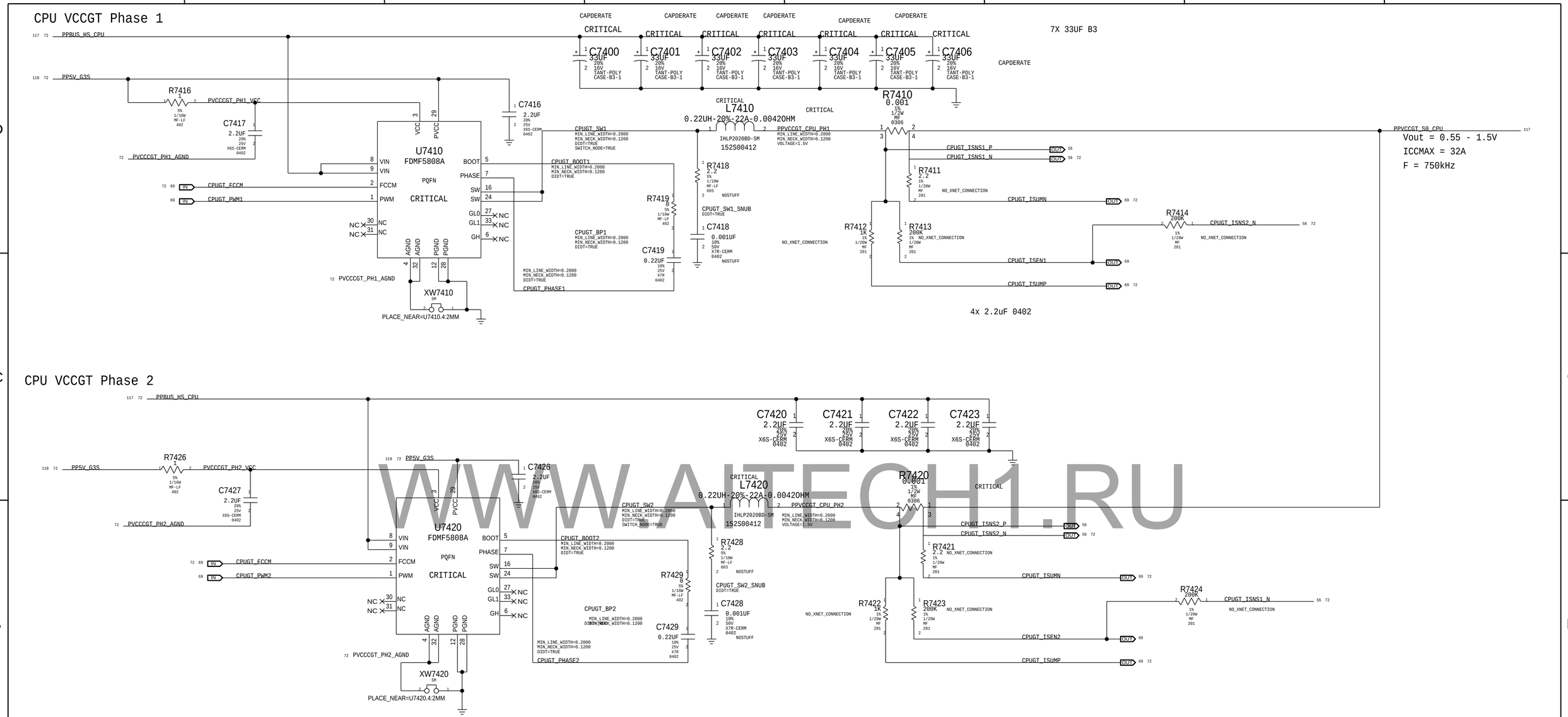

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PAGE TITLE

IMVP GT Block

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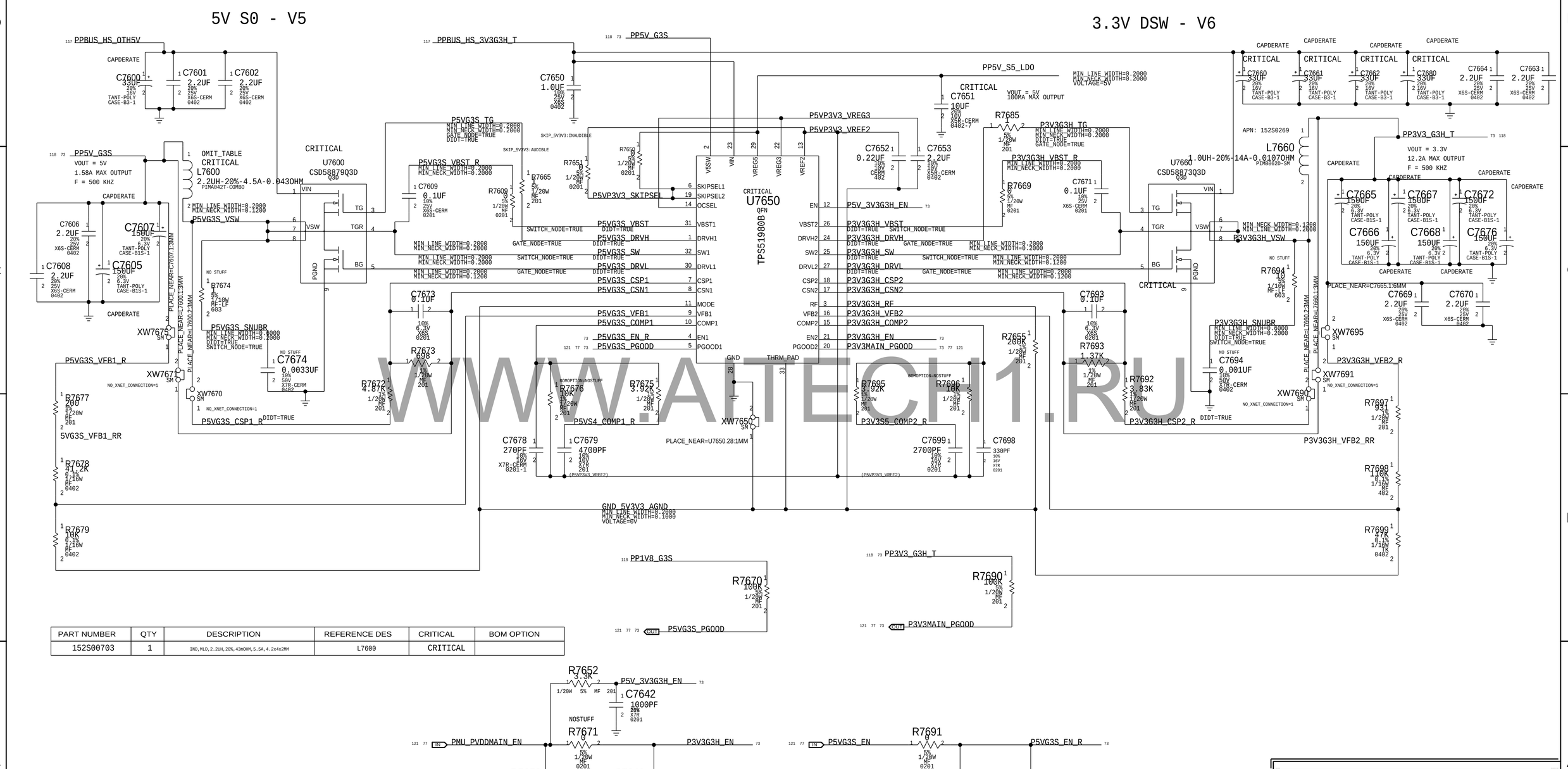

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00703	1	IND,MLD,2.2UH,20%,43mOHM,5.5A,4.2x4x2MM	L7600	CRITICAL	

PAGE TITLE
Power 5V 3.3V Supply

Apple Inc.

DRAWING NUMBER 051-04492
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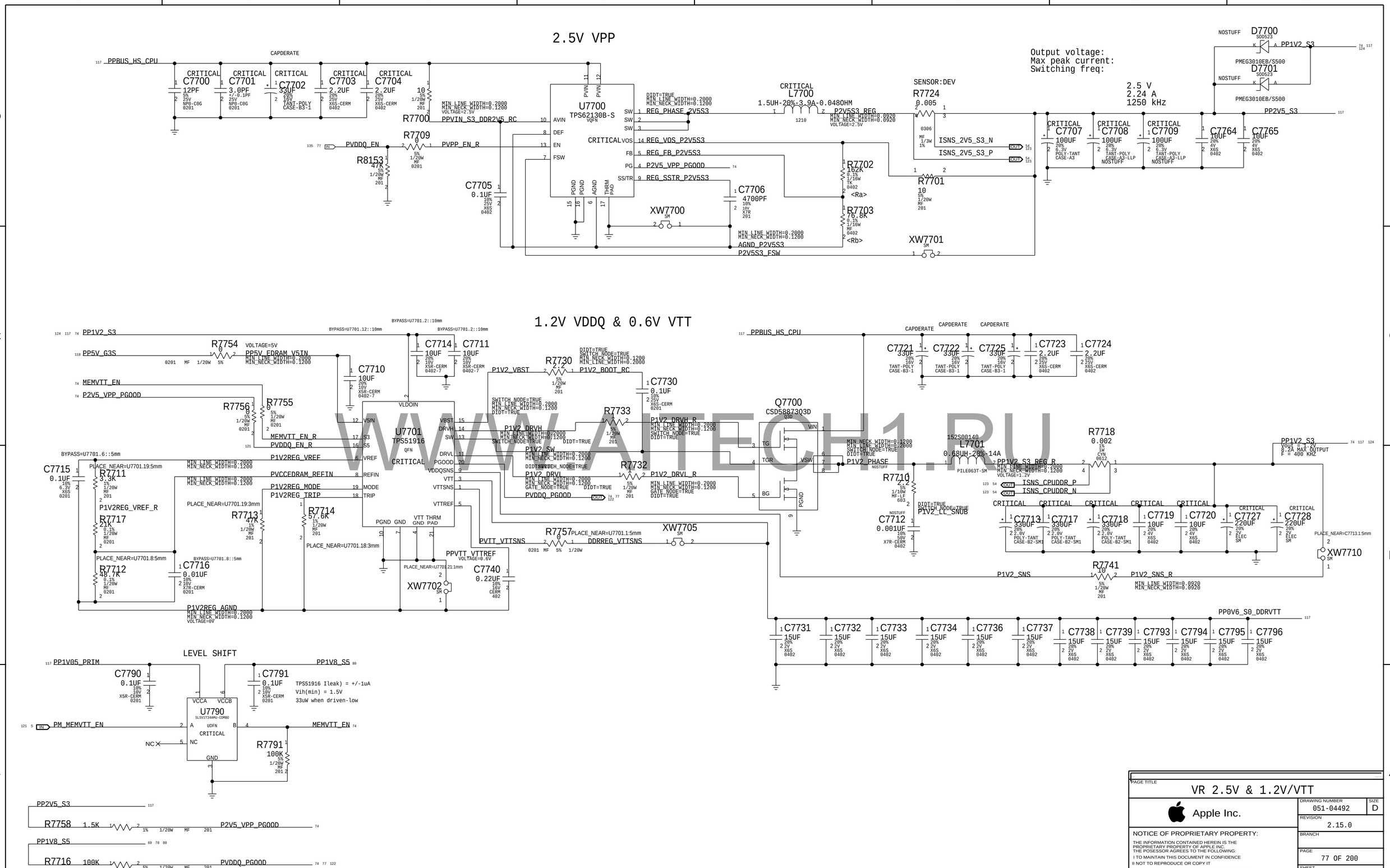

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PAGE TITLE
VR 2.5V & 1.2V/VTT

Apple Inc.

DRAWING NUMBER 051-04492
SIZE D
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BRANCH
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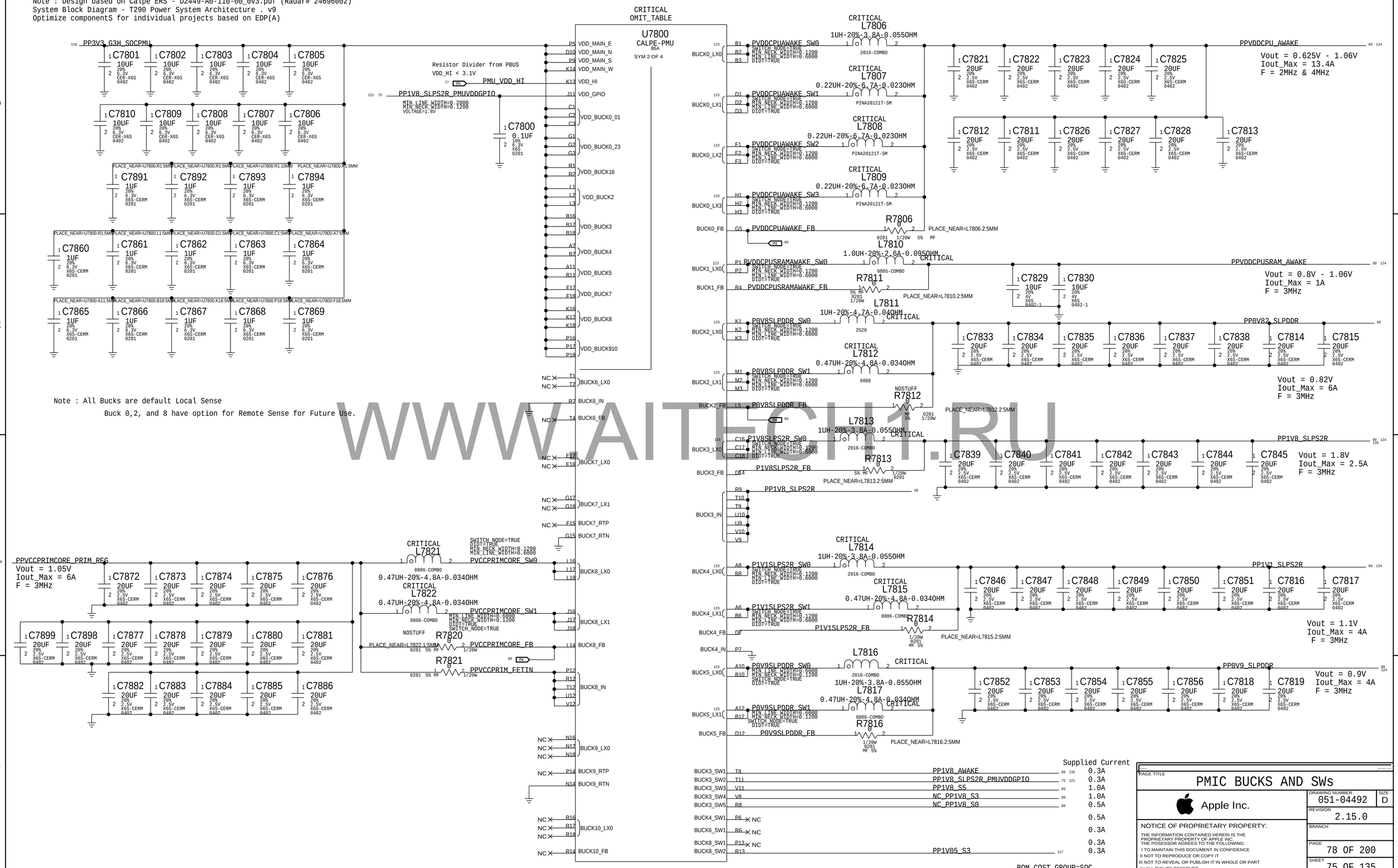
Note : Design based on Calpe ERS - D2449-A0-110-00_0v3.pdf (Radar# 24696002)
System Block Diagram - T290 Power System Architecture . v9
Optimize componentS for individual projects based on EDP(A)



Note : All Bucks are default Local Sense
Buck 0,2, and 8 have option for Remote Sense for Future Use.

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PAGE TITLE
PMIC BUCKS AND SWs

Apple Inc.

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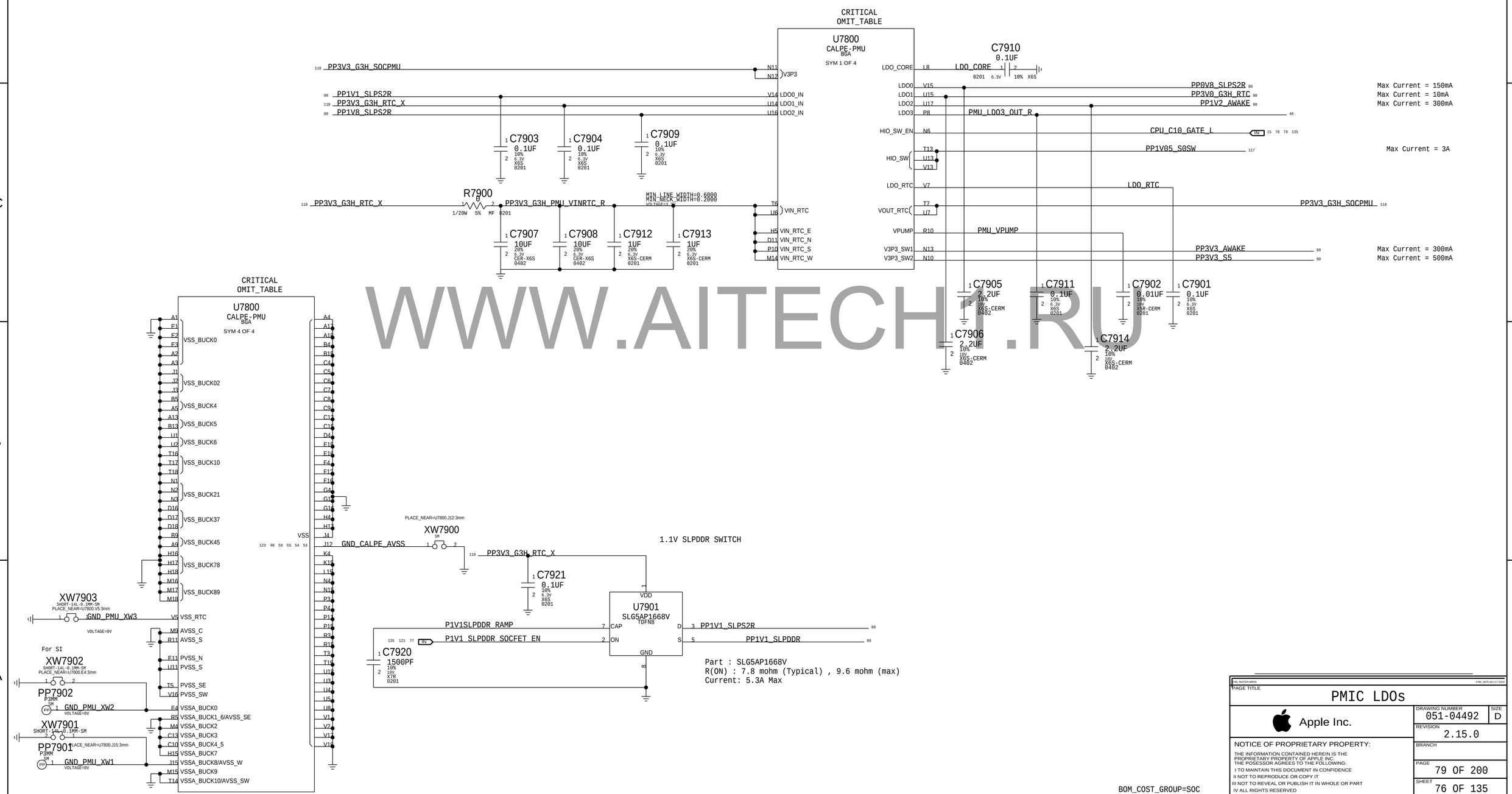

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PAGE TITLE

PMIC LDOs

Apple Inc.

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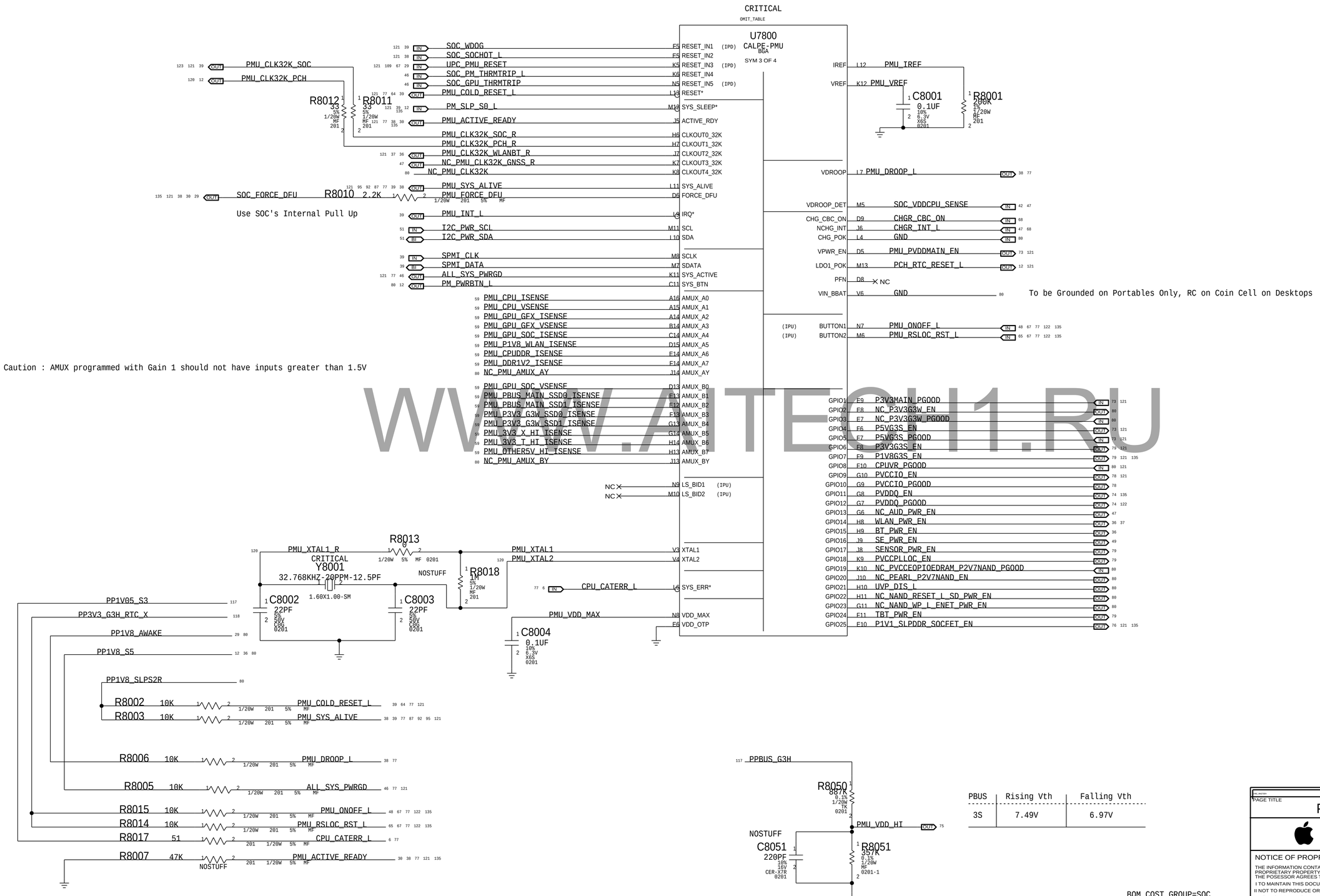

Caution : AMUX programmed with Gain 1 should not have inputs greater than 1.5V

PBUS	Rising Vth	Falling Vth
3S	7.49V	6.97V

BOM_COST_GROUP=SOC

PAGE TITLE

PMIC GPIOs & Control

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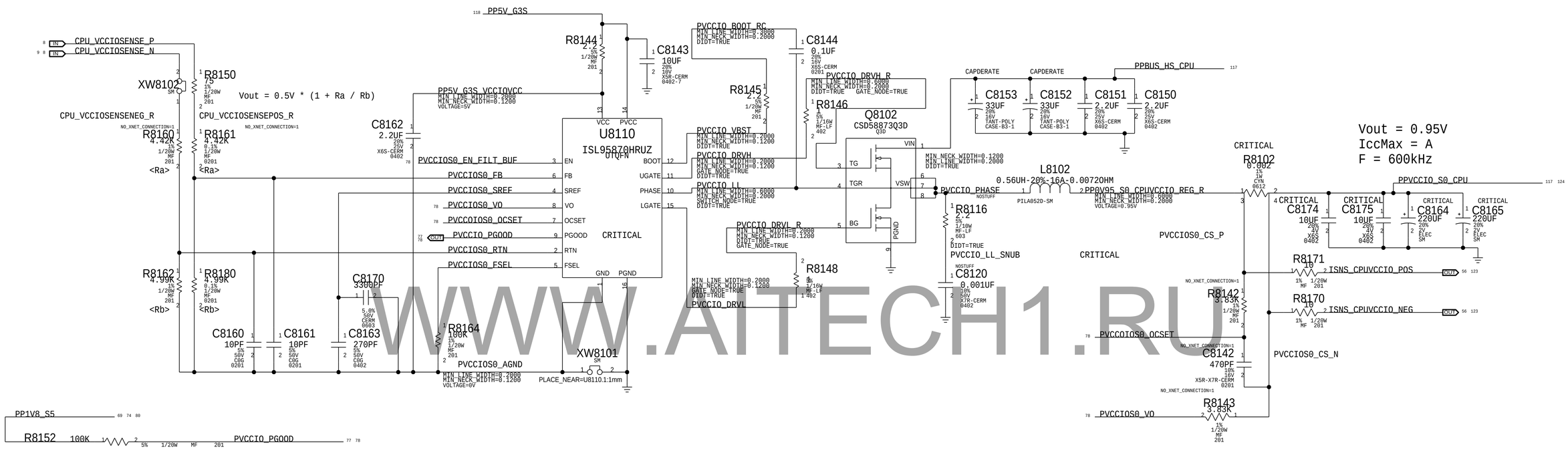
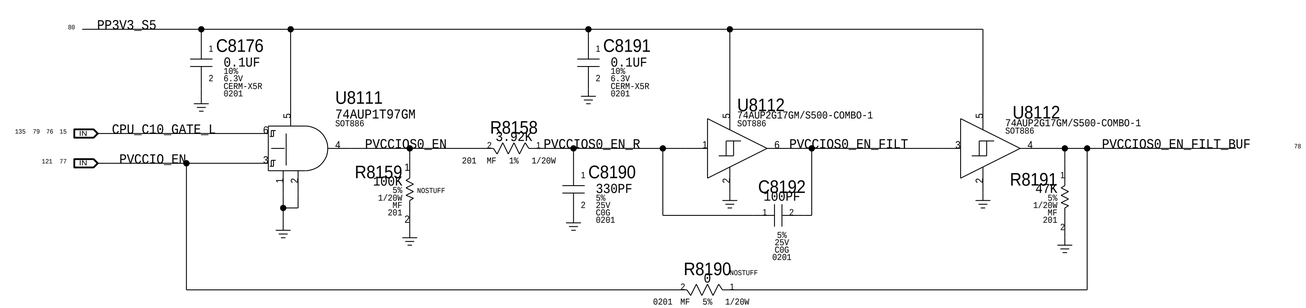
0.95V VCCIO



VCCIO ENABLE LOGIC



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BOM_COST_GROUP=PLATFORM POWER

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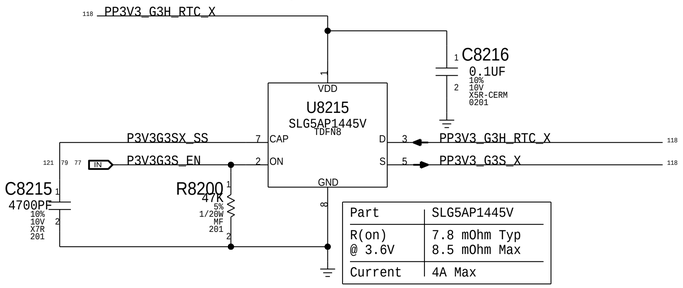
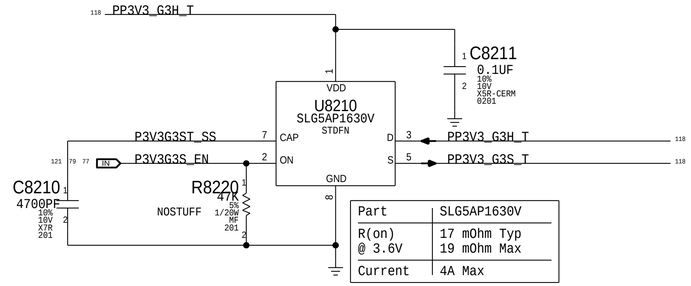
3.3V G3 Standby Switch X



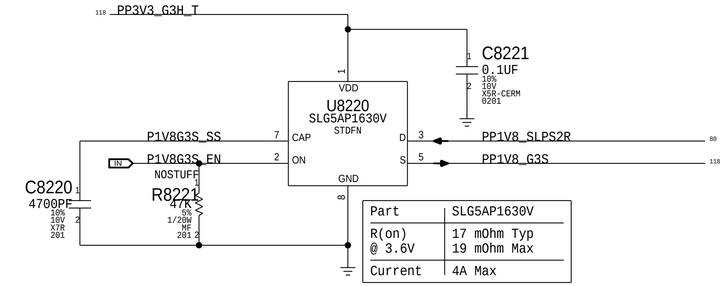
Part	SLG5AP1445V
R(on) @ 3.6V	7.8 mOhm Typ 8.5 mOhm Max
Current	4A Max

3.3V G3 Standby Switch T



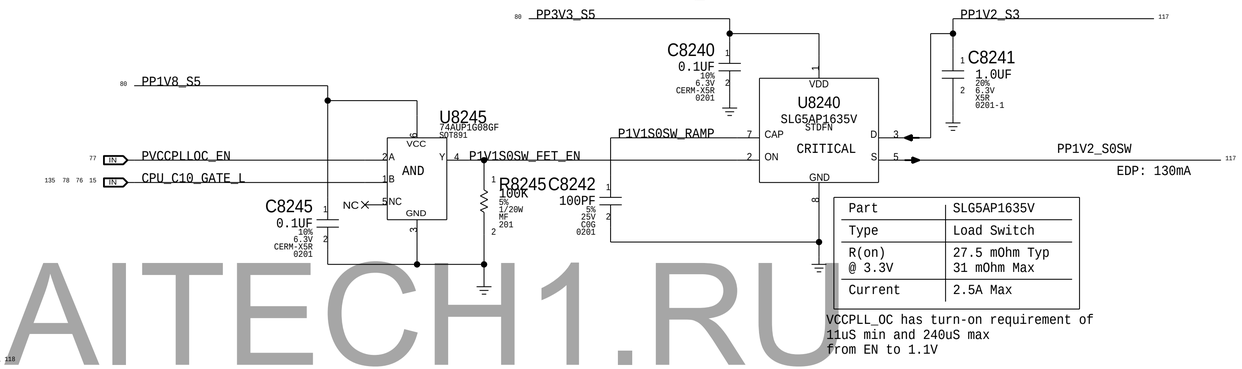
Part	SLG5AP1630V
R(on) @ 3.6V	17 mOhm Typ 19 mOhm Max
Current	4A Max

1.8V G3 Standby Switch



Part	SLG5AP1630V
R(on) @ 3.6V	17 mOhm Typ 19 mOhm Max
Current	4A Max

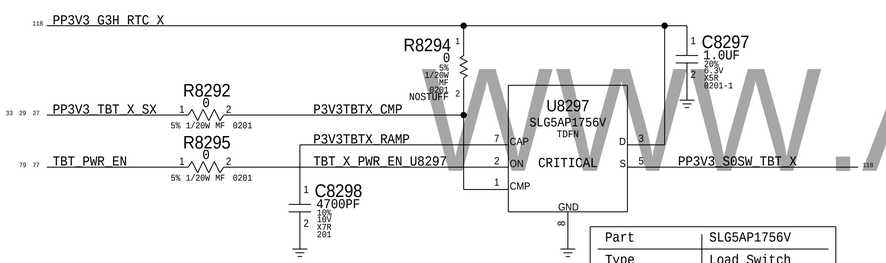
1.1V S0SW VCCPLL_OC Switch



Part	SLG5AP1635V
Type	Load Switch
R(on) @ 3.3V	27.5 mOhm Typ 31 mOhm Max
Current	2.5A Max

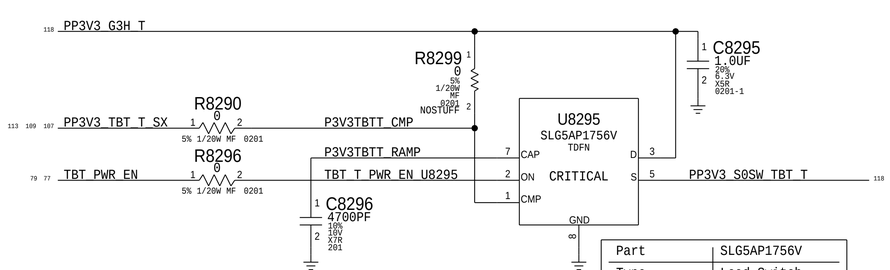
VCCPLL_OC has turn-on requirement of 11uS min and 240uS max from EN to 1.1V

3.3V S0SW TBT X Switch



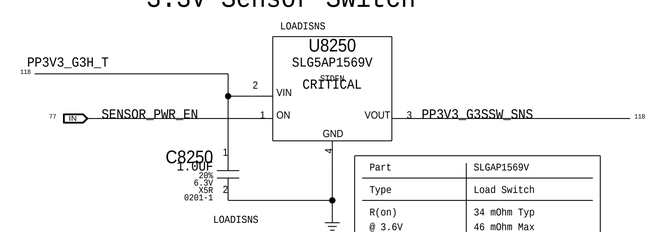
Part	SLG5AP1756V
Type	Load Switch
R(on) @ 4A	7.8 mOhm Typ 8.5 mOhm Max
Current	4A Max

3.3V S0SW TBT T Switch



Part	SLG5AP1756V
Type	Load Switch
R(on) @ 4A	7.8 mOhm Typ 8.5 mOhm Max
Current	4A Max

3.3V Sensor Switch



Part	SLGAP1569V
Type	Load Switch
R(on) @ 3.6V	34 mOhm Typ 46 mOhm Max
Current	1A Max

BOM_COST_GROUP=PLATFORM POWER

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Power FETs

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PMIC Buck0 - SoC VDD_CPU

```
124 75 PPVDDCPU_AWAKE ==
       PPVDDCPU_AWAKE
       MIN_LINE_WIDTH=0.4000
       MIN_NECK_WIDTH=0.1200
       VOLTAGE=1.05V
       MAKE_BASE=TRUE                    121 123
       ==
       PPVDDCPU_AWAKE                    42 80
```

PMIC Buck1 - SoC VDD_CPU_SRAM

```
124 75 PPVDDCPUSRAM_AWAKE ==
       PPVDDCPUSRAM_AWAKE
       MIN_LINE_WIDTH=0.4000
       MIN_NECK_WIDTH=0.1200
       VOLTAGE=1.05V
       MAKE_BASE=TRUE                    121
       ==
       PPVDDCPUSRAM_AWAKE                42
```

PMIC Buck2 - SoC VDD_SOC

```
75 PP0V82_SLPDDR ==
   PP0V82_SLPDDR
   MIN_LINE_WIDTH=0.7000
   MIN_NECK_WIDTH=0.1200
   VOLTAGE=0.82V
   MAKE_BASE=TRUE                        121 123
   ==
   PP0V82_SLPDDR                         42 80
```

PMIC BUCK3 - SoC AOP/SMC/VDD1

```
135 124 75 PP1V8_SLPS2R ==
           PP1V8_SLPS2R
           MIN_LINE_WIDTH=0.2000
           MIN_NECK_WIDTH=0.1200
           VOLTAGE=1.8V
           MAKE_BASE=TRUE                121 122 123
           ==
           PP1V8_SLPS2R                  75
           PP1V8_SLPS2R                  79
           PP1V8_SLPS2R                  76
           PP1V8_SLPS2R                  46
           PP1V8_SLPS2R                  77
           PP1V8_SLPS2R                  64
           PP1V8_SLPS2R                  46
           PP1V8_SLPS2R                  38 47
           PP1V8_SLPS2R                  44
           PP1V8_SLPS2R                  44
           PP1V8_SLPS2R                  44
           PP1V8_SLPS2R                  44
           PP1V8_SLPS2R                  68
           PP1V8_SLPS2R                  51
           PP1V8_SLPS2R                  51
           PP1V8_SLPS2R                  51
           PP1V8_SLPS2R                  47
           PP1V8_SLPS2R                  29 30 31 110 111
           PP1V8_SLPS2R
           PP1V8_SLPS2R                  135
           PP1V8_SLPS2R
           PP1V8_SLPS2R
           PP1V8_SLPS2R                  48
           PP1V8_SLPS2R                  47
```

PMIC BUCK3 SW 1

```
135 75 PP1V8_AWAKE ==
       PP1V8_AWAKE                       66 121
       MIN_LINE_WIDTH=0.2000   VOLTAGE=1.8V
       MIN_NECK_WIDTH=0.1200   MAKE_BASE=TRUE
       ==
       PP1V8_AWAKE                       29 77
       PP1V8_AWAKE                       46
       PP1V8_AWAKE                       44
       PP1V8_AWAKE                       44
       PP1V8_AWAKE                       44
       PP1V8_AWAKE                       44
       PP1V8_AWAKE                       44
       PP1V8_AWAKE                       41 46 47
       PP1V8_AWAKE                       46
       PP1V8_AWAKE
       PP1V8_AWAKE
```

PMIC BUCK3 SW 3

```
75 PP1V8_S5 ==
   PP1V8_S5                              121
   MIN_LINE_WIDTH=0.2000
   MIN_NECK_WIDTH=0.1200
   VOLTAGE=1.8V
   MAKE_BASE=TRUE
   ==
   PP1V8_S5                              46
   PP1V8_S5                              16 17
   PP1V8_S5                              39
   PP1V8_S5                              12 16
   PP1V8_S5                              12 13 15 16 19 20 52
   PP1V8_S5                              15
   PP1V8_S5
   PP1V8_S5                              17
   PP1V8_S5
   PP1V8_S5                              12 36 77
   PP1V8_S5                              51
   PP1V8_S5                              51
   PP1V8_S5                              51
   PP1V8_S5                              46
   PP1V8_S5
   PP1V8_S5
   PP1V8_S5                              69 74 78
   PP1V8_S5                              95
   PP1V8_S5                              79
   PP1V8_S5                              74
   PP1V8_S5                              16
   PP1V8_S5                              57
   PP1V8_S5                              57
   PP1V8_S5                              57
   PP1V8_S5                              46
   PP1V8_S5                              18
```

PMIC BUCK3 SW 4/5

```
75 NC_PP1V8_S3 ==
   NC_PP1V8_S3
   MAKE_BASE=TRUE

75 NC_PP1V8_S0 ==
   NC_PP1V8_S0
   MAKE_BASE=TRUE
```

PMIC Buck4 - SDRAM VDD2

```
124 75 PP1V1_SLPS2R ==
       PP1V1_SLPS2R
       MIN_LINE_WIDTH=0.5000
       MIN_NECK_WIDTH=0.1200
       VOLTAGE=1.1V
       MAKE_BASE=TRUE                    121
       ==
       PP1V1_SLPS2R                      76
       PP1V1_SLPS2R                      76
       PP1V1_SLPS2R                      43
       PP1V1_SLPS2R                      44
```

Buck 4 Ext. SW U7901 - VDDIO_DDR & PLL

```
76 PP1V1_SLPDDR ==
   PP1V1_SLPDDR                          121
   MIN_LINE_WIDTH=0.2000
   MIN_NECK_WIDTH=0.1200
   VOLTAGE=1.1V
   MAKE_BASE=TRUE
   ==
   PP1V1_SLPDDR                          38
   PP1V1_SLPDDR                          43
   PP1V1_SLPDDR                          43
   PP1V1_SLPDDR                          44
```

PMIC Buck5 - VDD_FIXED

```
124 75 PP0V9_SLPDDR ==
       PP0V9_SLPDDR                      121
       MIN_LINE_WIDTH=0.3000
       MIN_NECK_WIDTH=0.1200
       VOLTAGE=0.9V
       MAKE_BASE=TRUE
       ==
       PP0V9_SLPDDR                      43
       PP0V9_SLPDDR                      43
       PP0V9_SLPDDR                      43
       PP0V9_SLPDDR                      43
       PP0V9_SLPDDR                      43
```

PMIC LDO0 - VDD_LOW

```
76 PP0V8_SLPS2R ==
   PP0V8_SLPS2R                          121
   MIN_LINE_WIDTH=0.2000
   MIN_NECK_WIDTH=0.1200
   VOLTAGE=0.8V
   MAKE_BASE=TRUE
   ==
   PP0V8_SLPS2R                          43
```

PMIC LDO2 - PCIE_REFBUF/PLL

```
76 PP1V2_AWAKE ==
   PP1V2_AWAKE                           121
   MIN_LINE_WIDTH=0.2000
   MIN_NECK_WIDTH=0.1200
   VOLTAGE=1.2V
   MAKE_BASE=TRUE
   ==
   PP1V2_AWAKE                           44
   PP1V2_AWAKE                           44
   PP1V2_AWAKE                           44
   PP1V2_AWAKE                           44
```

PMIC V3P3 SW 1 - USB

```
76 PP3V3_AWAKE ==
   PP3V3_AWAKE                           121
   MIN_LINE_WIDTH=0.2000
   MIN_NECK_WIDTH=0.1200
   VOLTAGE=3.3V
   MAKE_BASE=TRUE
   ==
   PP3V3_AWAKE                           44
```

PMIC V3P3 SW 2 (Internal) -

```
76 PP3V3_S5 ==
   PP3V3_S5                              121
   MIN_LINE_WIDTH=0.6000
   MIN_NECK_WIDTH=0.1500
   VOLTAGE=3.3V
   MAKE_BASE=TRUE
   ==
   PP3V3_S5                              12 16 17
   PP3V3_S5                              46
   PP3V3_S5                              78
   PP3V3_S5                              15 16 19
   PP3V3_S5                              14 16
   PP3V3_S5                              15 16
   PP3V3_S5                              18
   PP3V3_S5                              20
   PP3V3_S5                              12 16 17
   PP3V3_S5                              79
   PP3V3_S5                              12 29
   PP3V3_S5                              95 115 126
   PP3V3_S5                              135
   PP3V3_S5                              16
   PP3V3_S5                              47
   PP3V3_S5
```

PMIC LDO 1 - PCH VCCRTC

```
76 PP3V0_G3H_RTC ==
   PP3V0_G3H_RTC                         121
   MIN_LINE_WIDTH=0.2000
   MIN_NECK_WIDTH=0.1200
   VOLTAGE=3.0V
   MAKE_BASE=TRUE
   ==
   PP3V0_G3H_RTC                         12 16 17
```

NC Aliases

```
77 NC_PVCCEOPIOEDRAM_P2V7NAND_PGOOD ==  MAKE_BASE  NC_PVCCEOPIOEDRAM_P2V7NAND_PGOOD
77 NC_PEARL_P2V7NAND_EN ==              MAKE_BASE  NC_PEARL_P2V7NAND_EN
77 UVP_DIS_L ==                         MAKE_BASE  UVP_DIS_L                          47
77 NC_NAND_RESET_L_SD_PWR_EN ==         MAKE_BASE  NC_NAND_RESET_L_SD_PWR_EN
77 NC_NAND_WP_L_ENET_PWR_EN ==          MAKE_BASE  NC_NAND_WP_L_ENET_PWR_EN
77 NC_P3V3G3W_PGOOD ==                  MAKE_BASE  NC_P3V3G3W_PGOOD
77 NC_P3V3G3W_EN ==                     MAKE_BASE  NC_P3V3G3W_EN
```

Alternate Feedback Sesne

```
                                NOSTUFF
                                R8320
                                0
75 OUT PVDDCPUAWAKE_FB          1  2  PVDDCPUAWAKE_FB_R        XW8320  1  2  PPVDDCPU_AWAKE   42 80
       Buck0 - Remote                 5%                                SM
                                      1/16W                             PLACE_NEAR=U3900.AA12:4MM
                                      MF-LF
                                      402
                                PLACE_NEAR=R7806.1:5MM

                                R8321
                                0
75 OUT P0V8SLPDDR_FB            1  2  P0V8SLPDDR_FB_R          XW8321  1  2  PP0V82_SLPDDR   42 80
       Buck2 - Remote                 5%                                SM
                                      1/16W                             PLACE_NEAR=U3900.AA20:6MM
                                      MF-LF
                                      402
                                PLACE_NEAR=R7812.1:5MM

                                R8322
                                0
75 OUT PVCCPRIMCORE_FB          1  2  PVCCPRIMCORE_FB_R       XW8322  1  2  PP1V05_PRIM    16 17 117
       Buck8 - Remote                 5%                                SM
                                      1/16W                             PLACE_NEAR=U1200.AB12:4MM
                                      MF-LF
                                      402
                                PLACE_NEAR=R7820.2:5MM
```

```
                                NC_CHGR_AUX_OK          MAKE_BASE  NC_CHGR_AUX_OK     68
121 18                          PM_PWRBTN_L             MAKE_BASE  PM_PWRBTN_L        12 77
121 77                          CPUVR_PGOOD             MAKE_BASE  CPUVR_PGOOD        69
46 8                            CPU_VCCST_PWRGD         MAKE_BASE  CPU_VCCST_PWRGD    69
                                NC_PMU_CLK32K           MAKE_BASE  NC_PMU_CLK32K      77
                                NC_PMU_AMUX_BY          MAKE_BASE  NC_PMU_AMUX_BY     77
                                NC_PMU_AMUX_AY          MAKE_BASE  NC_PMU_AMUX_AY     77
                                                        MAKE_BASE
```

```
77 GND ==  MAKE_BASE
77 GND ==  MAKE_BASE
```

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SOC/PMIC Aliases

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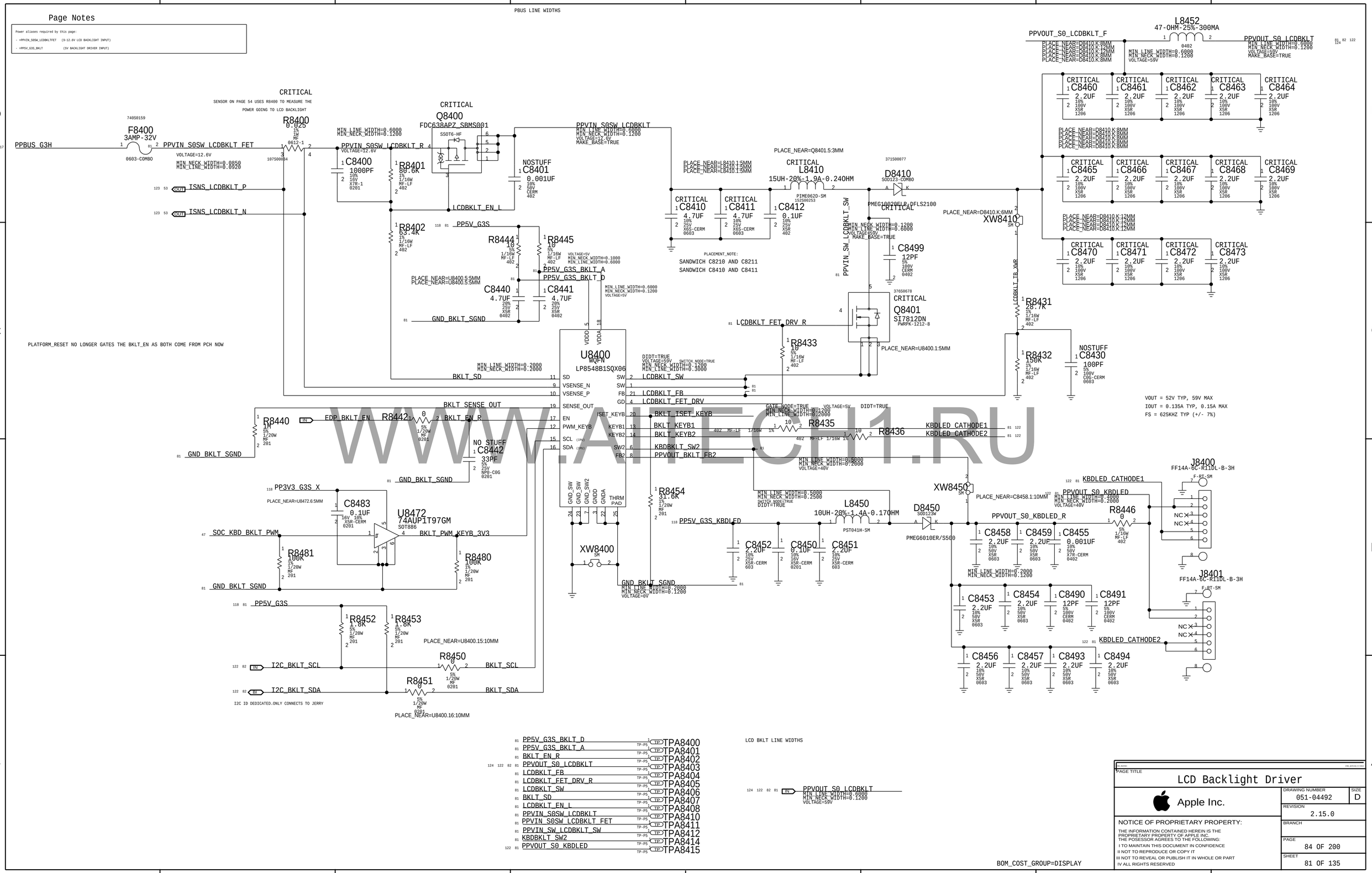

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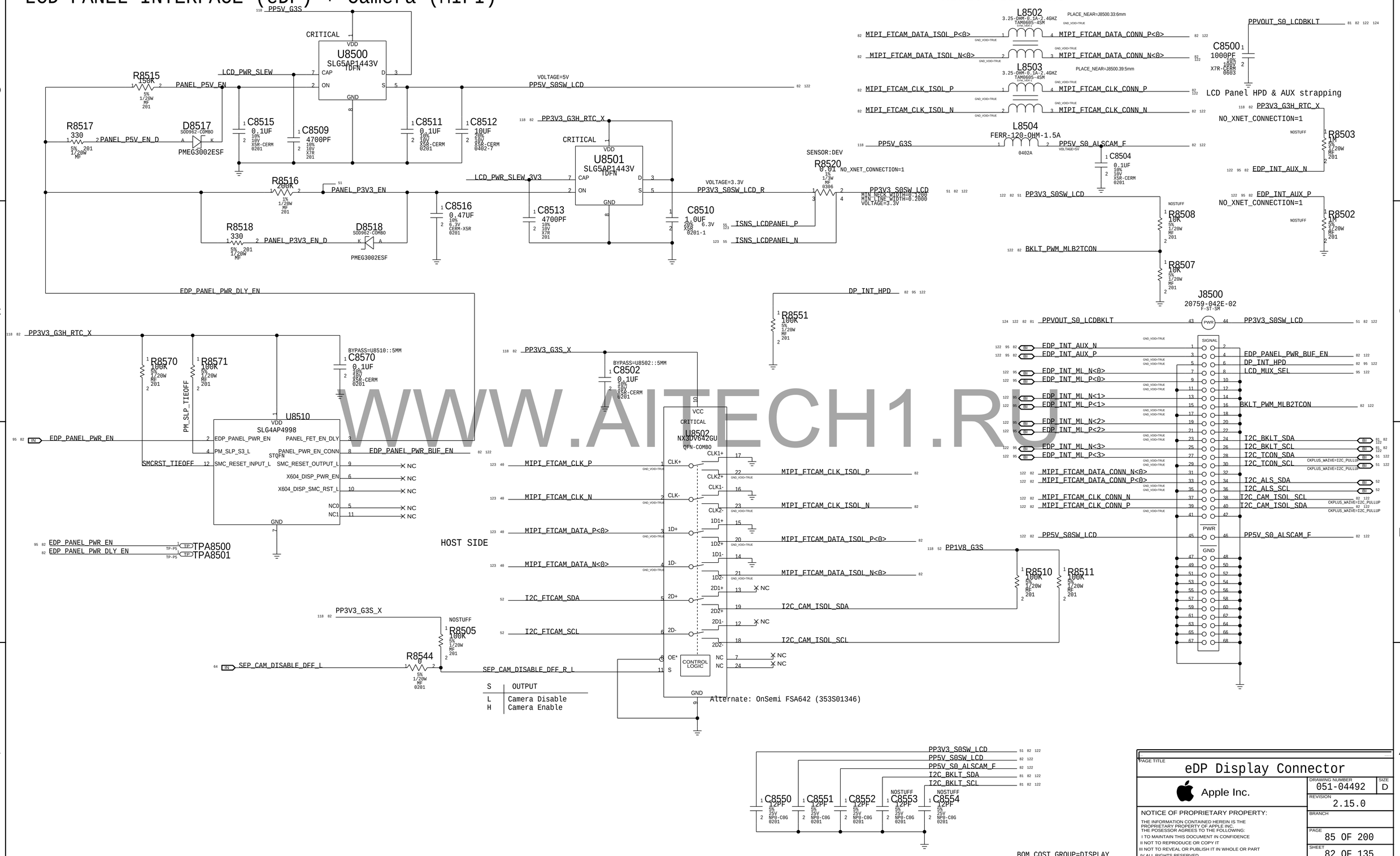
LCD PANEL INTERFACE (eDP) + Camera (MIPI)



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PAGE TITLE
eDP Display Connector

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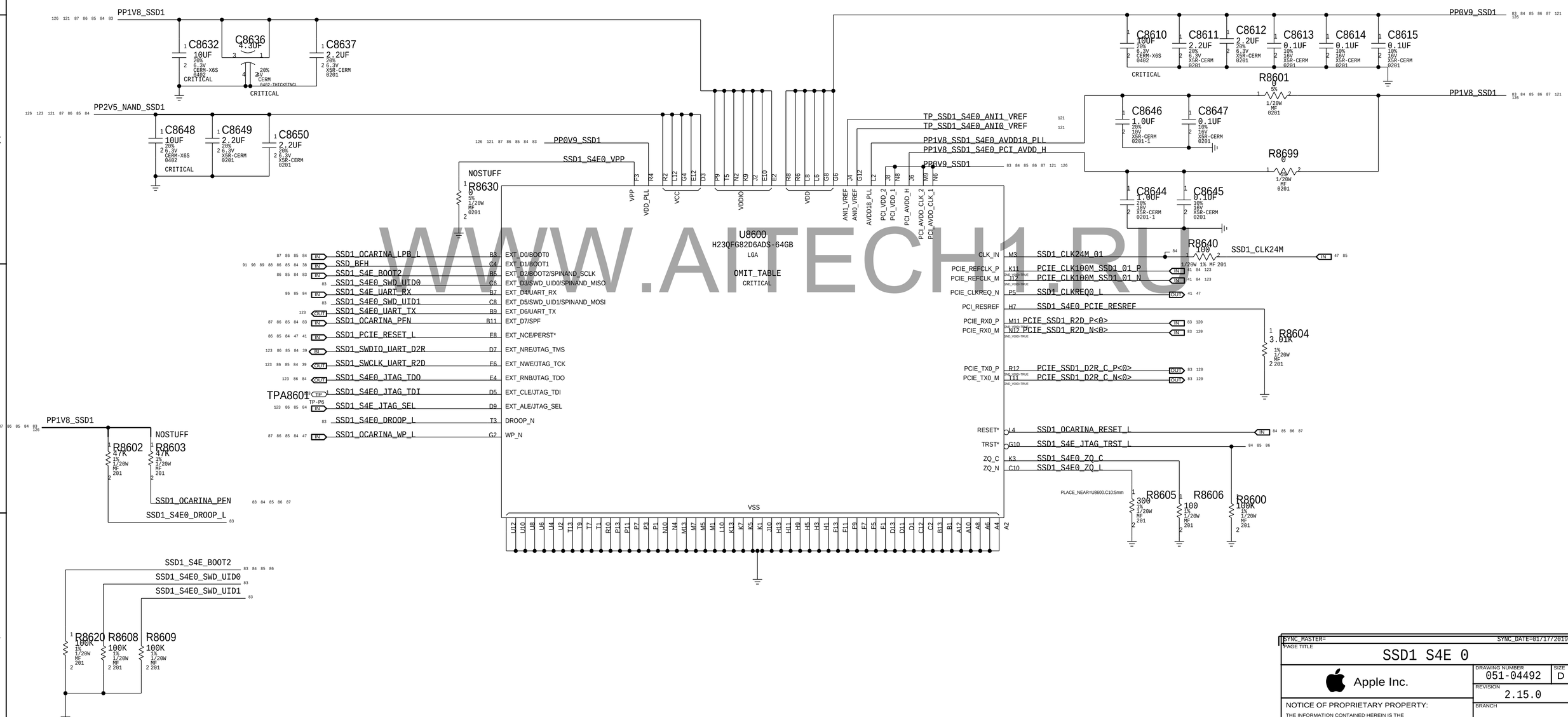
S4E0



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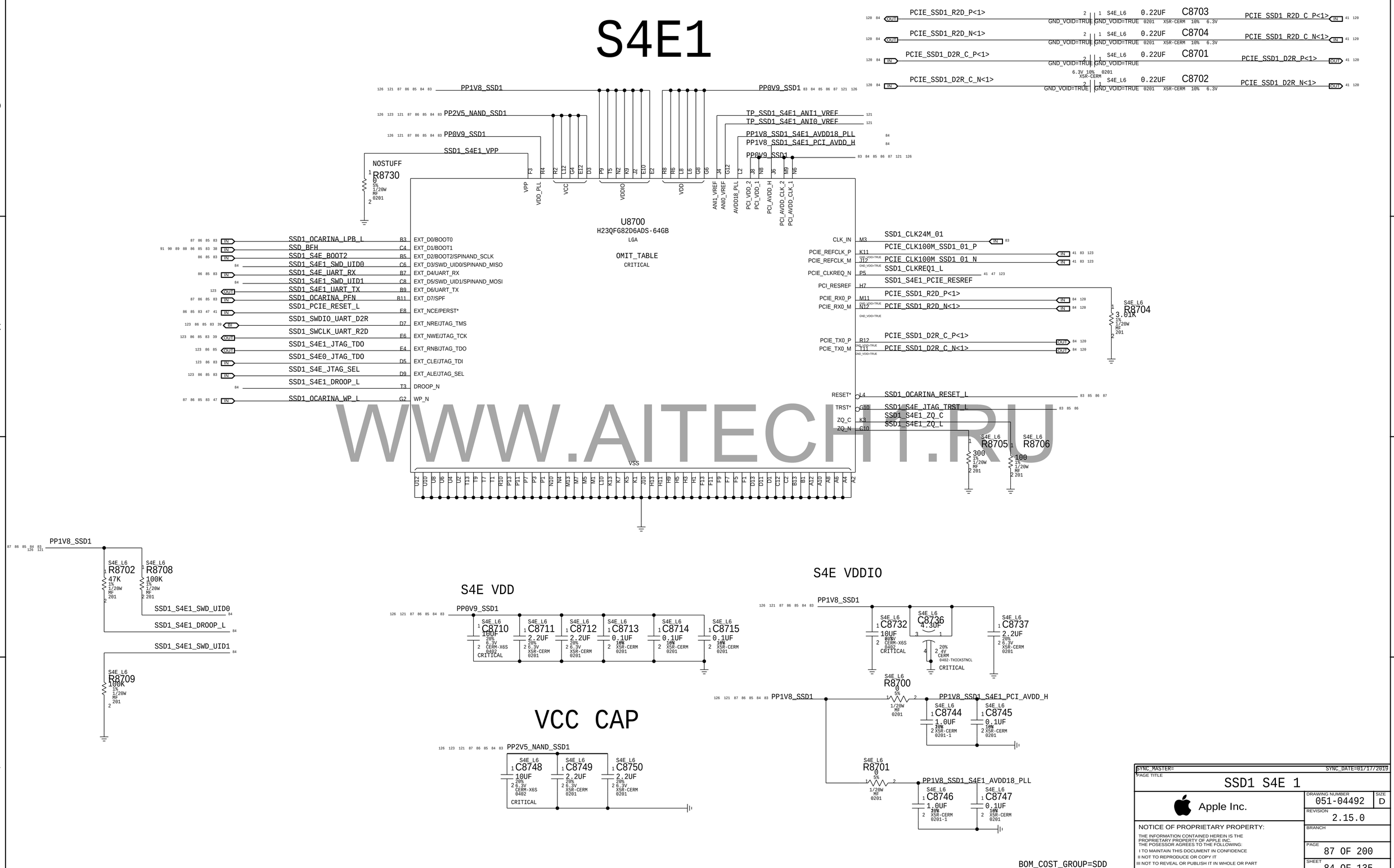
S4E1



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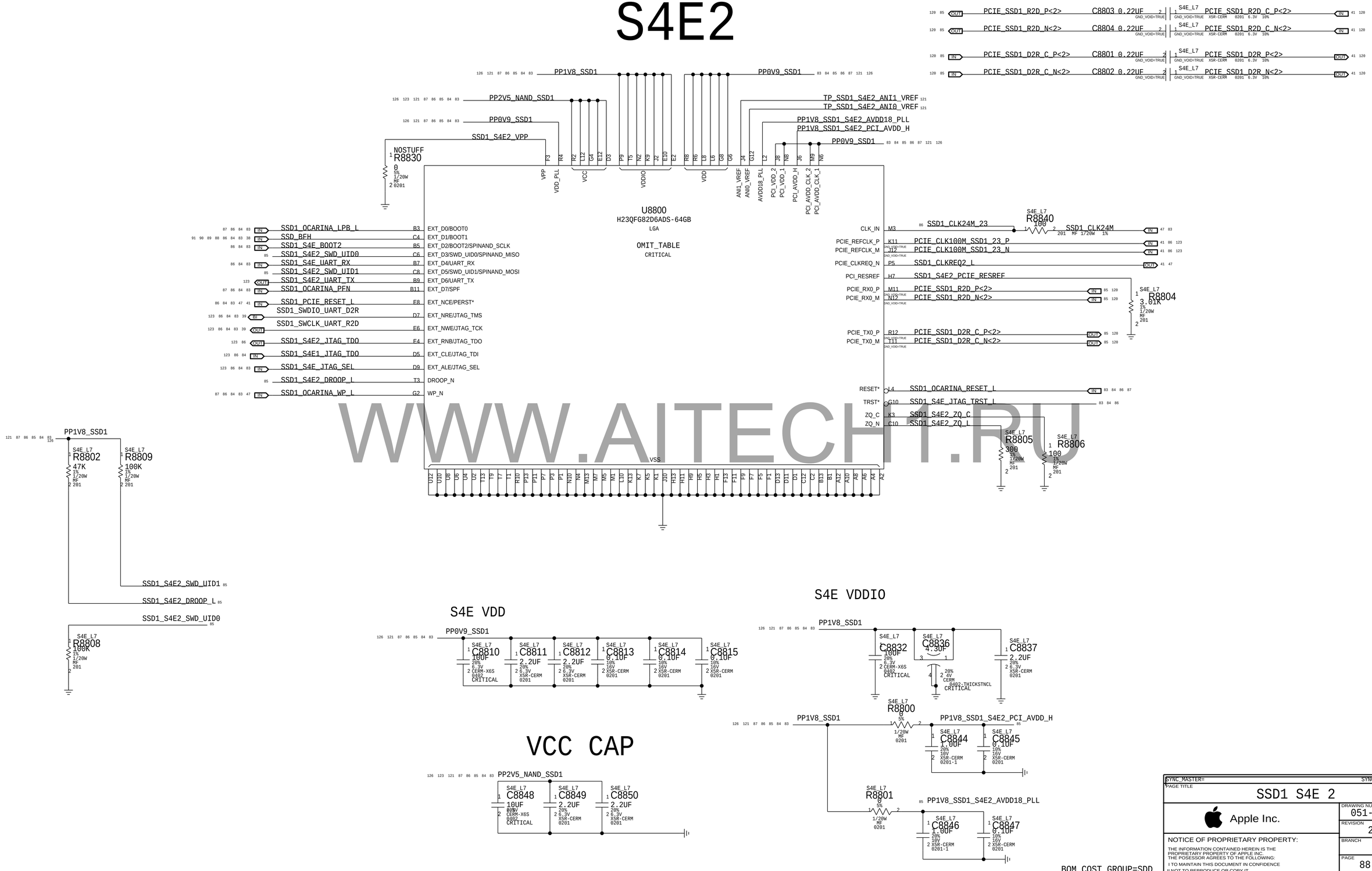
S4E2



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PAGE TITLE

SSD1 S4E 2

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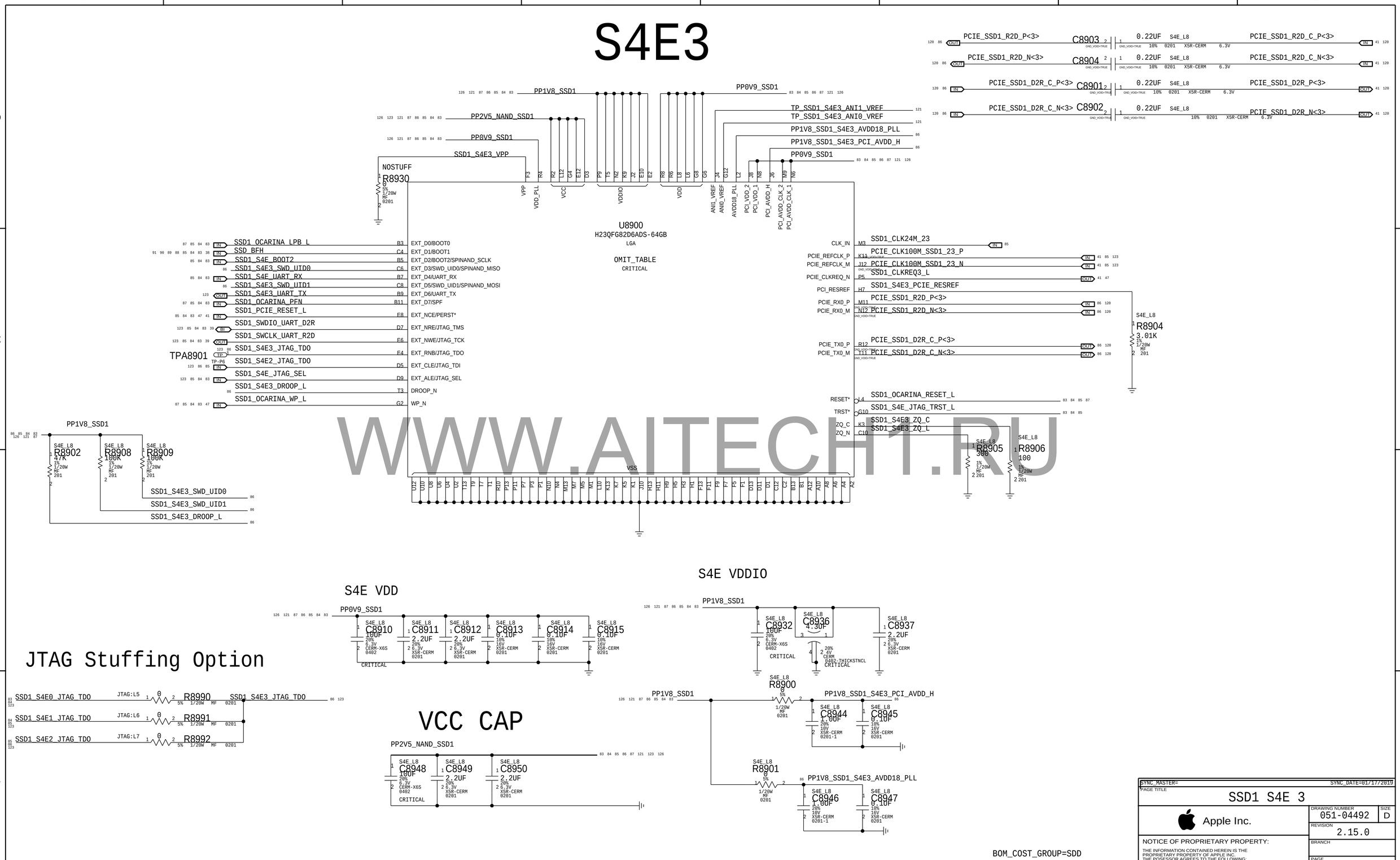

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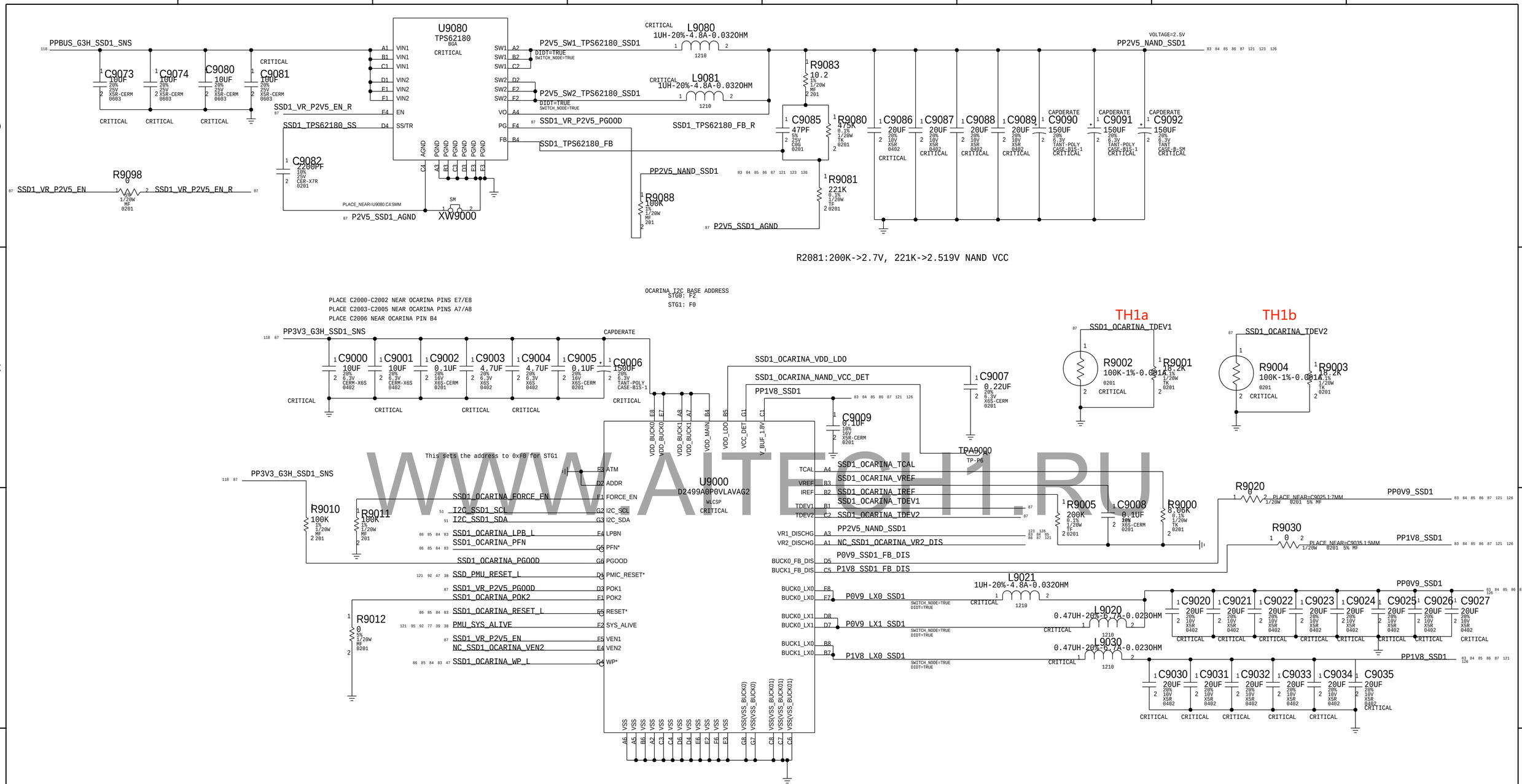

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PAGE TITLE: SSD1 PMIC & VR

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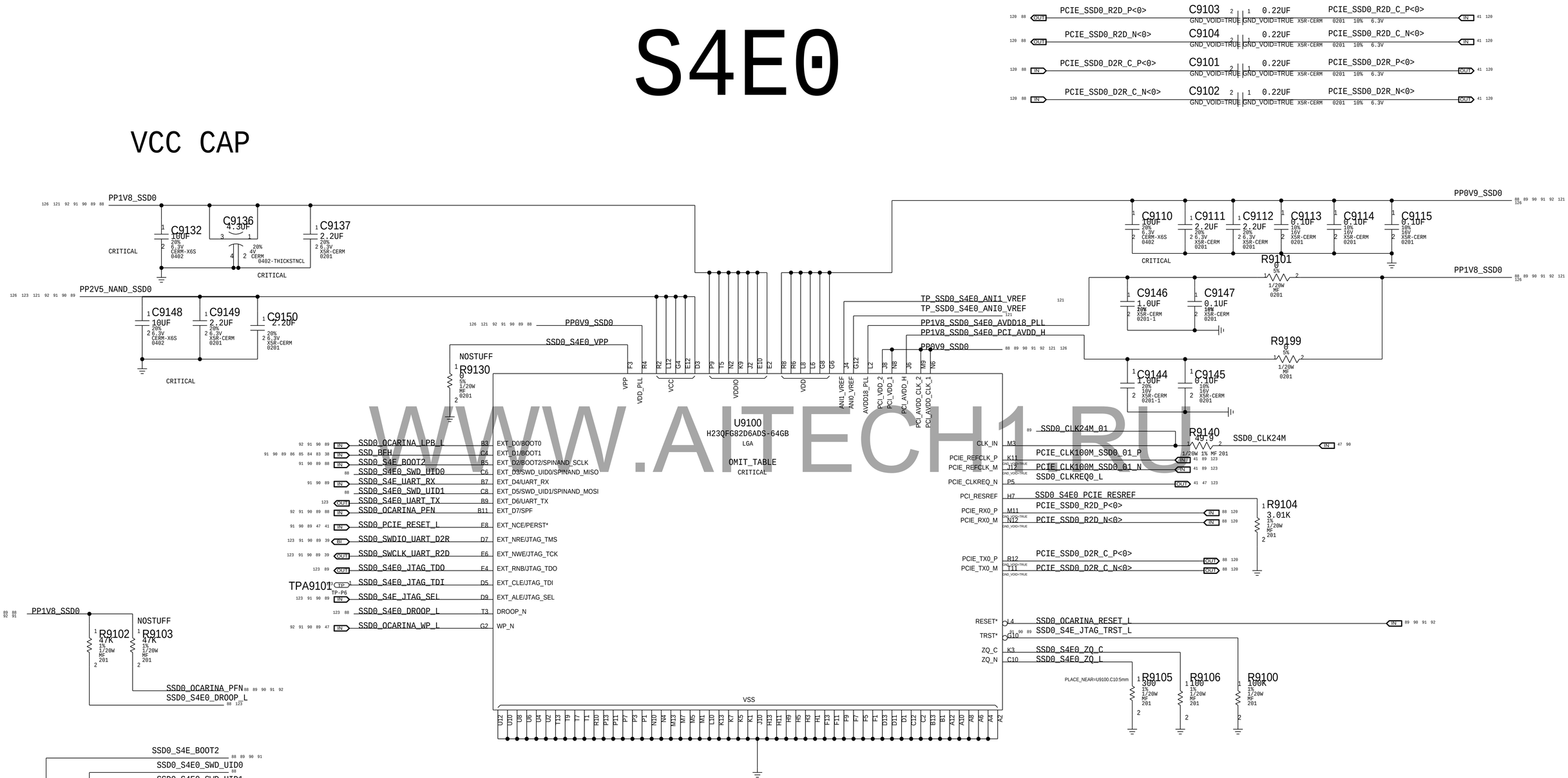

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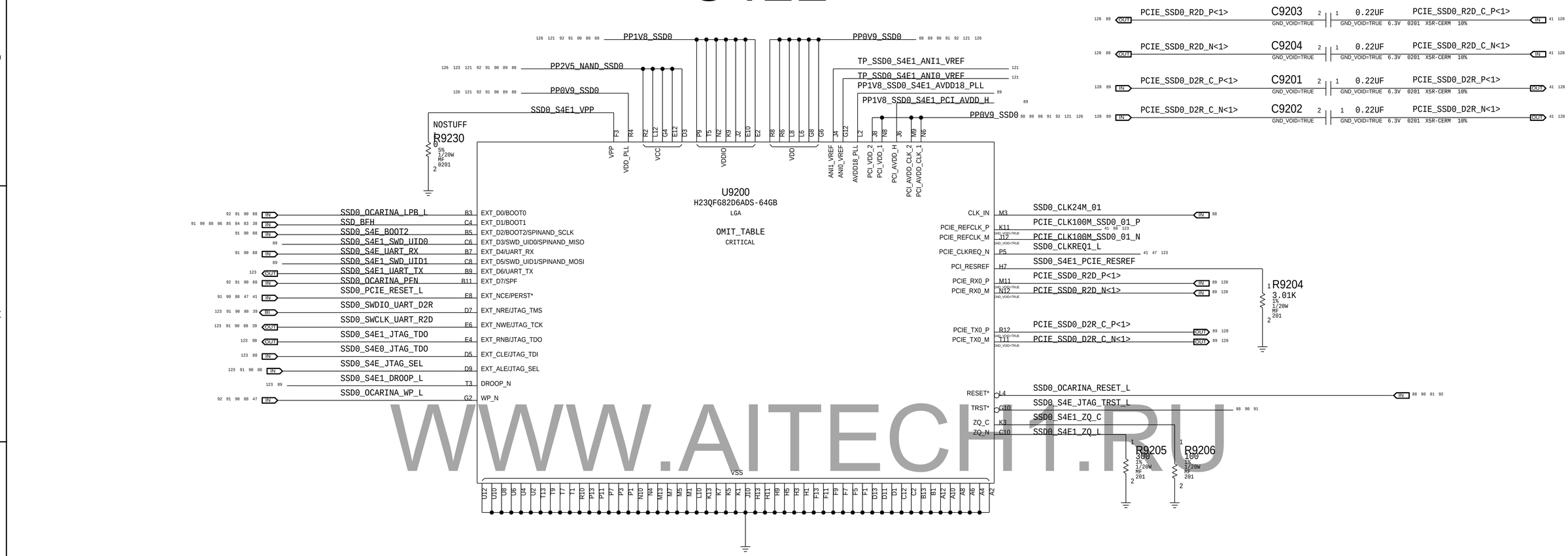

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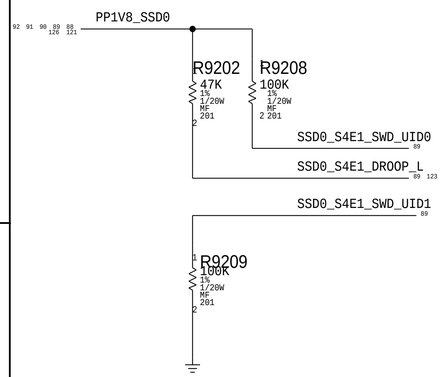

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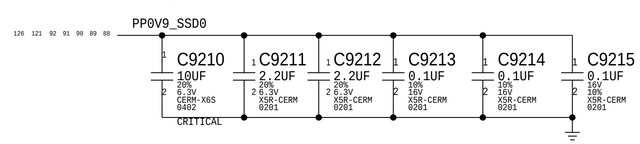

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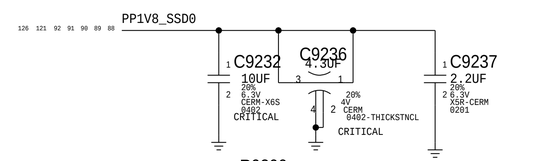

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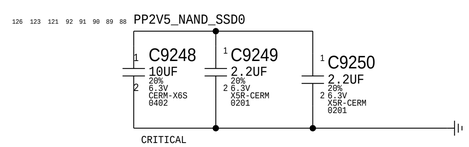

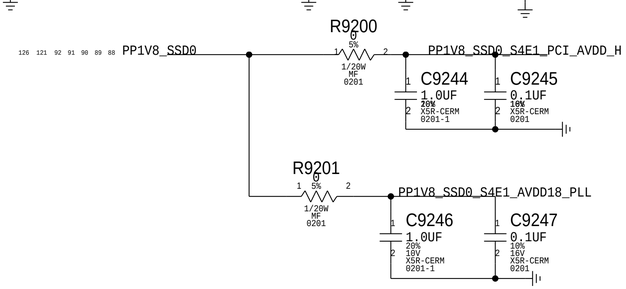

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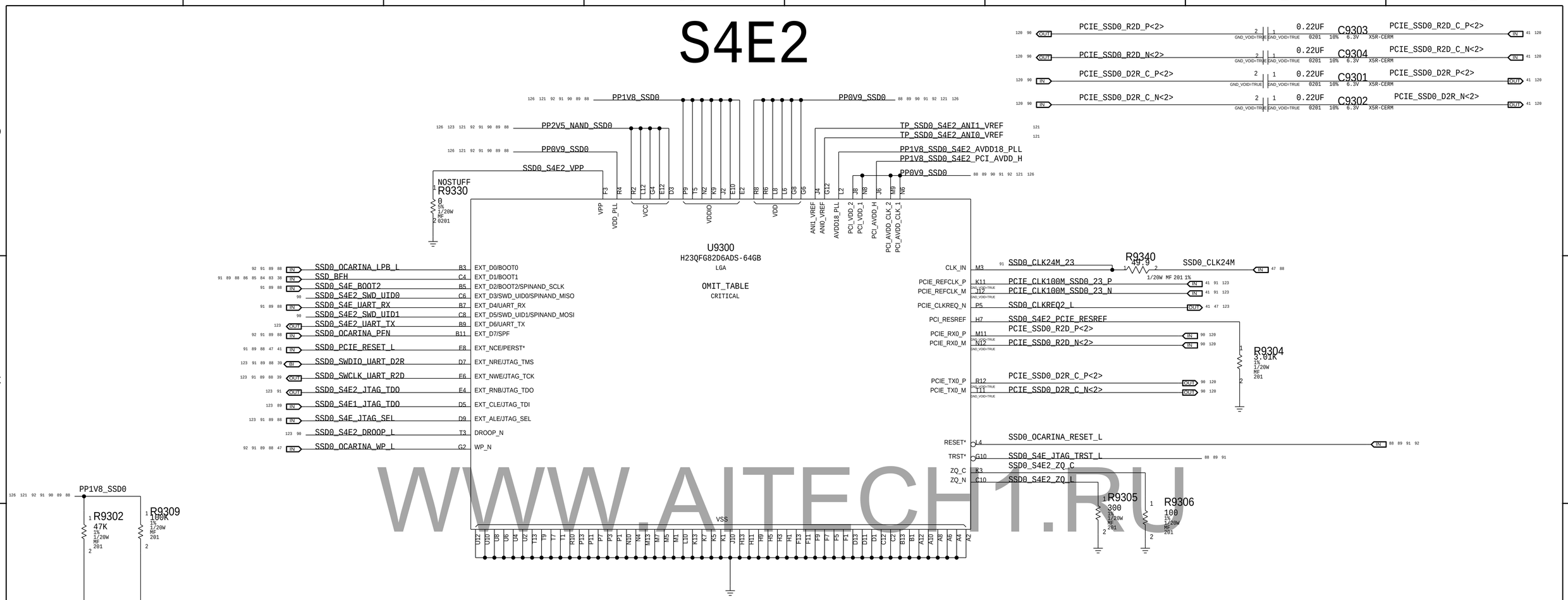

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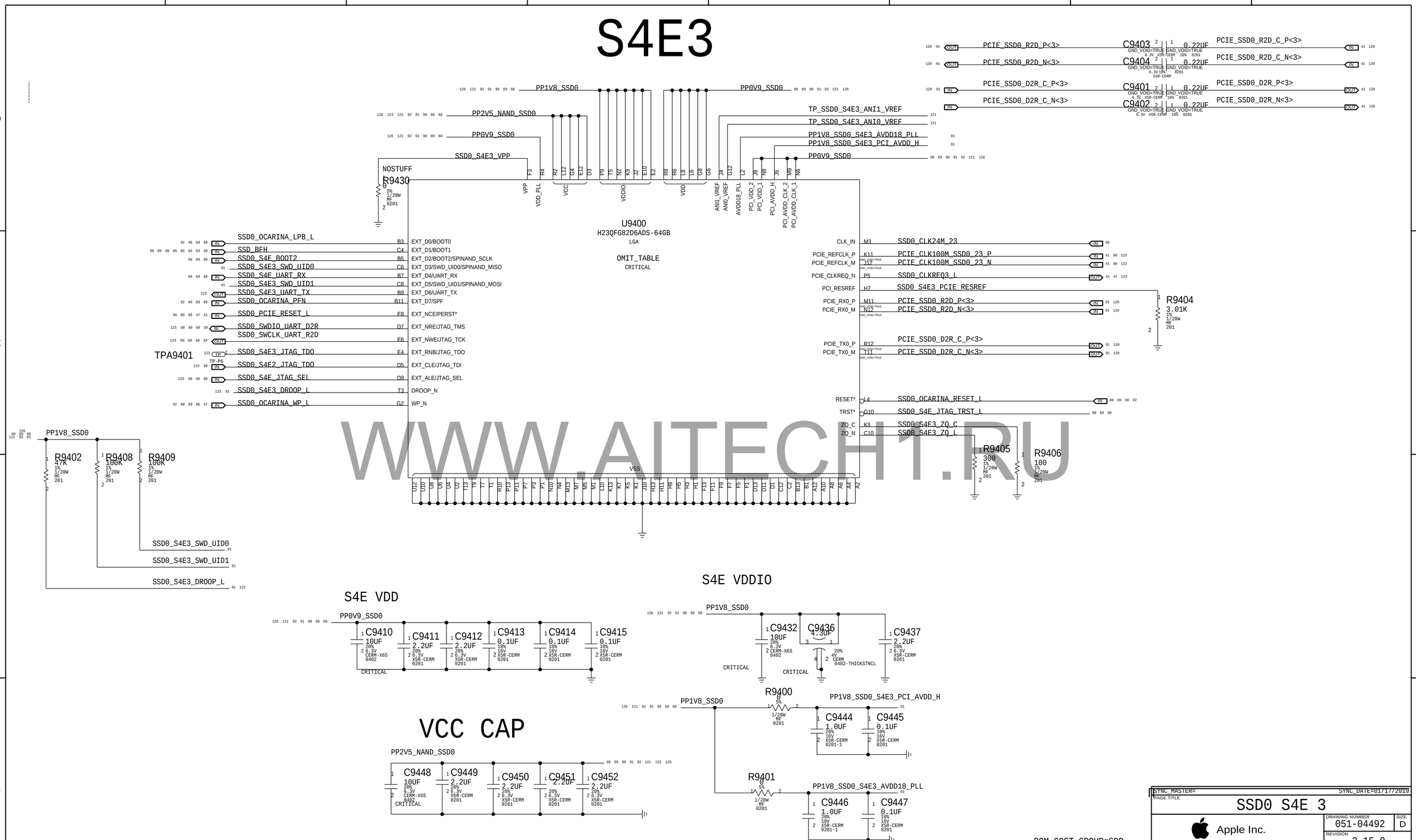

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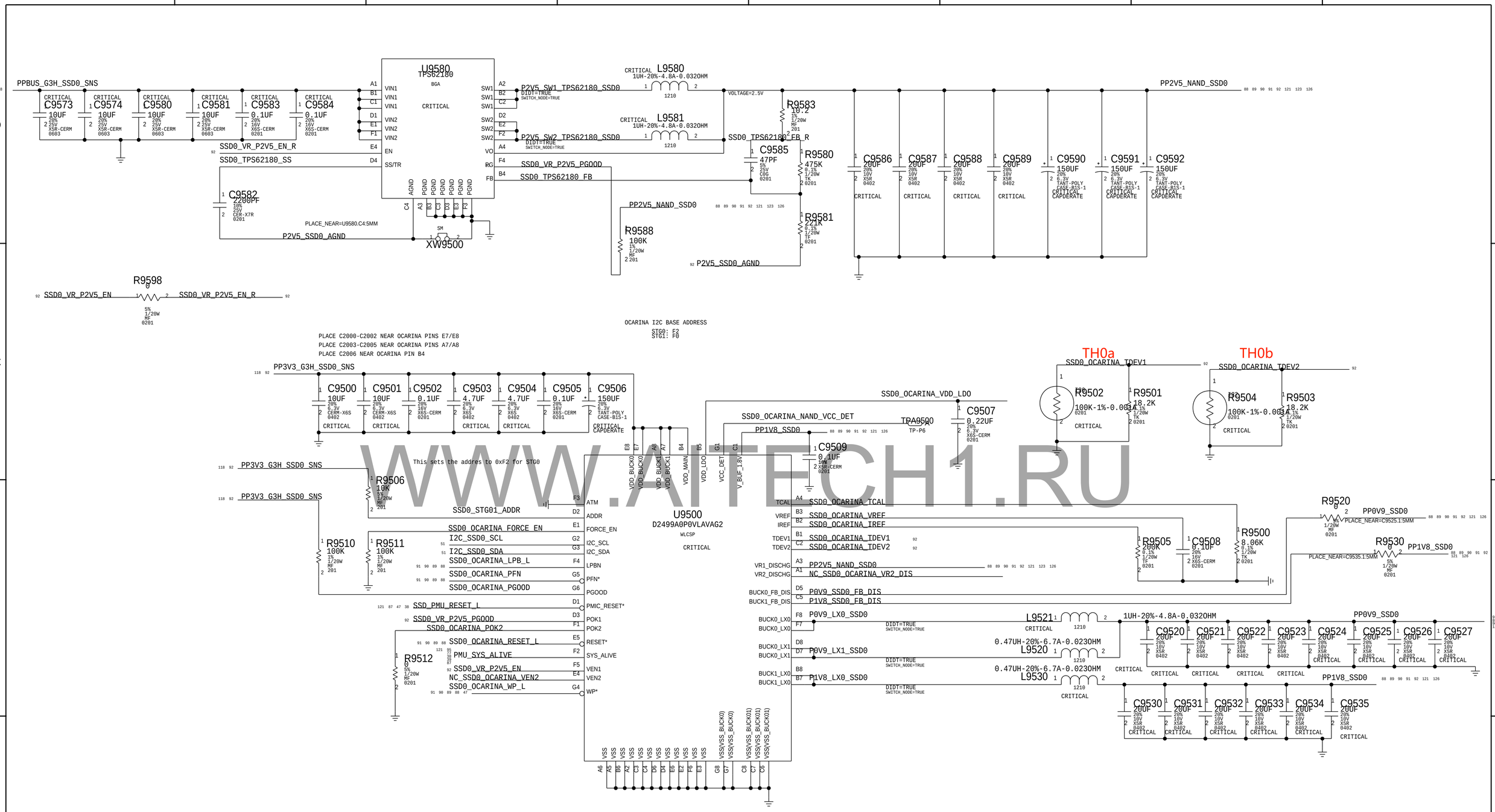

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PAGE TITLE: SSD0 PMIC & VR

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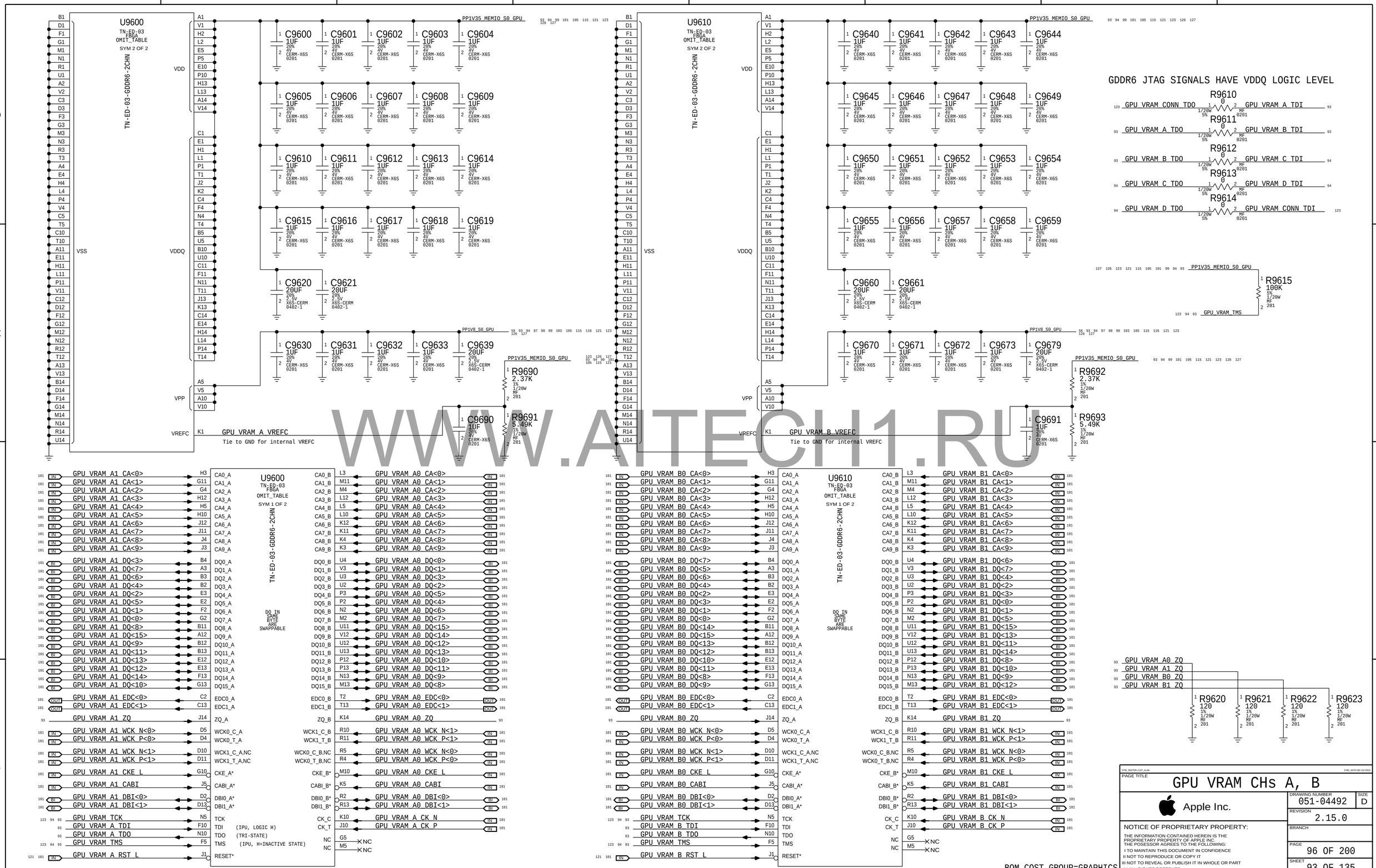

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PAGE TITLE
GPU VRAM CHs A, B

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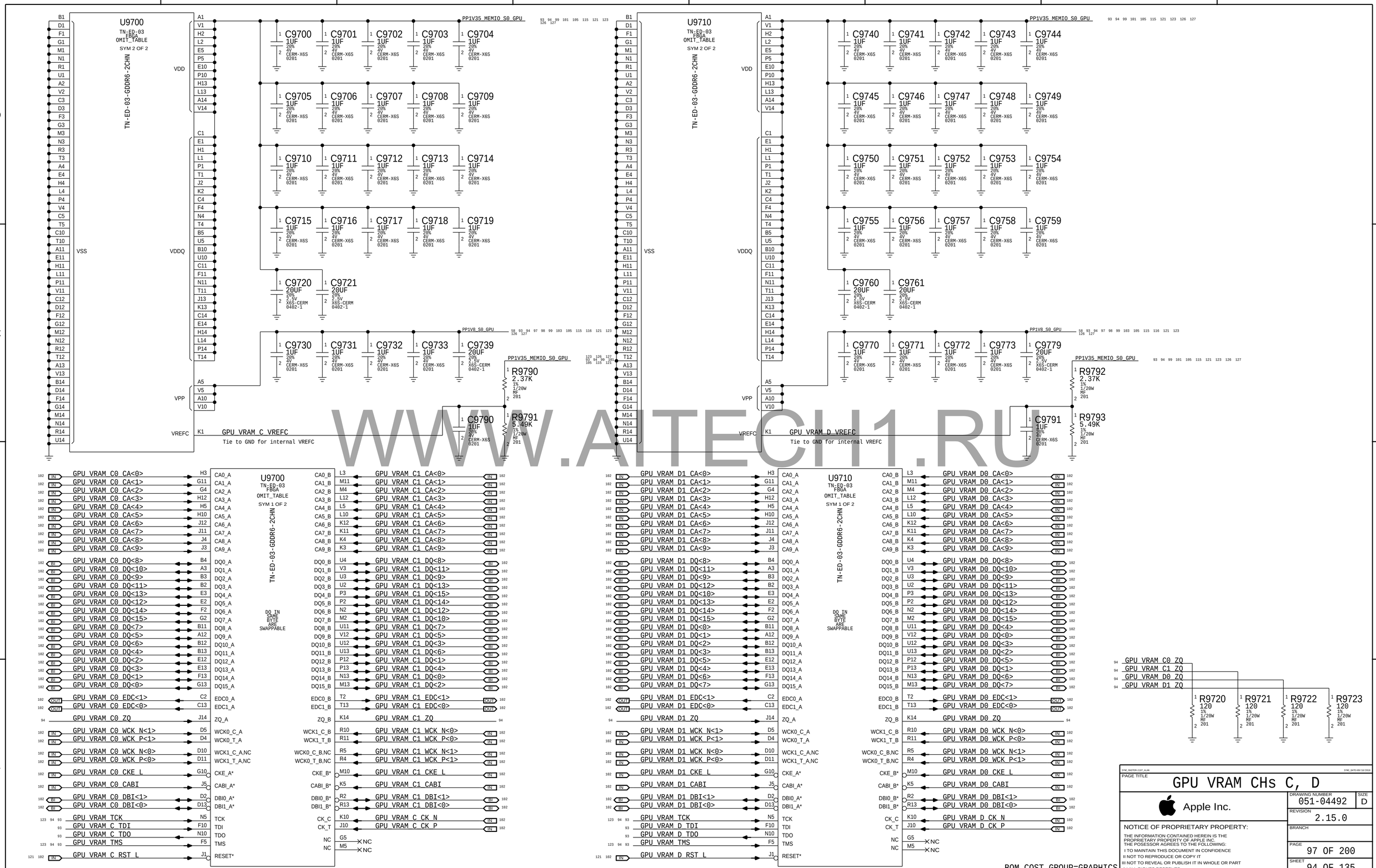

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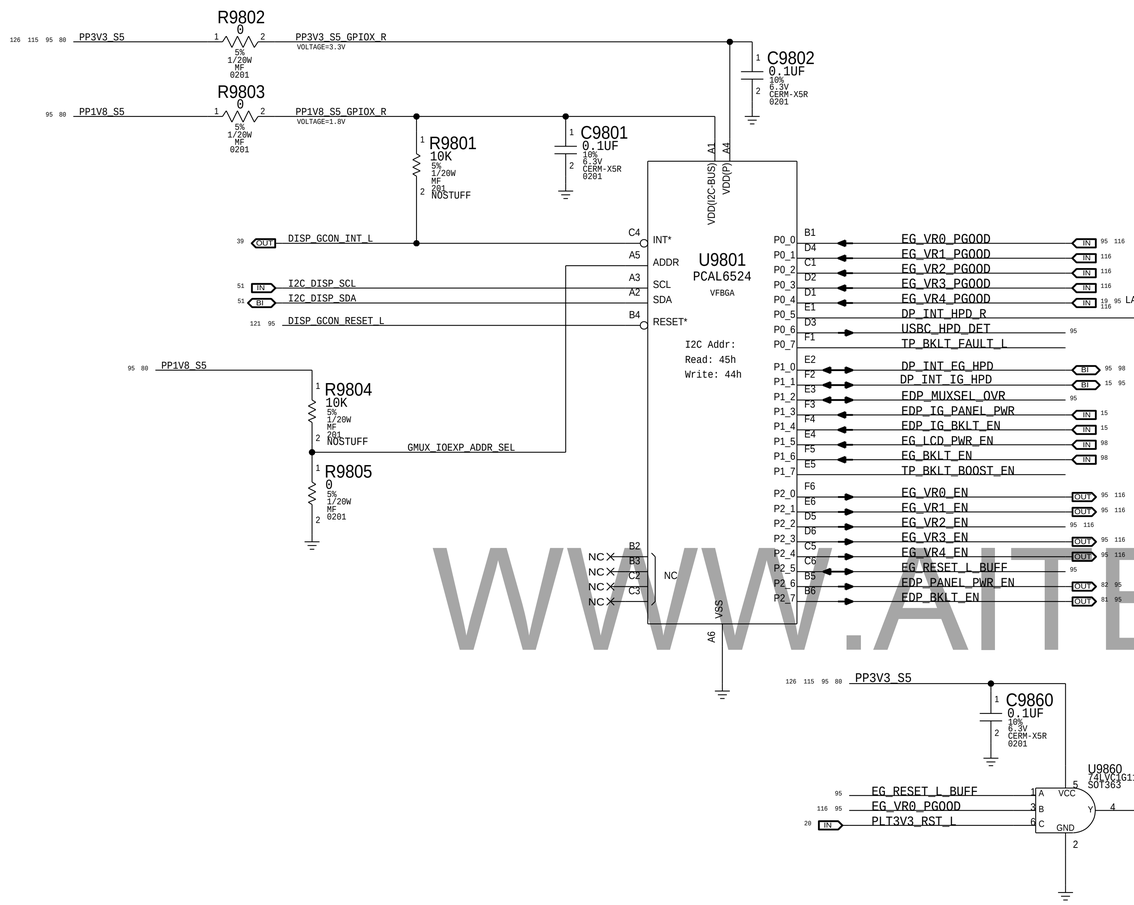

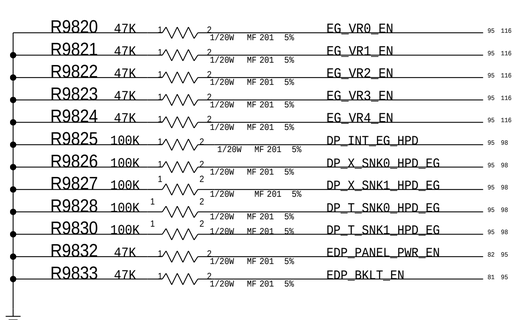

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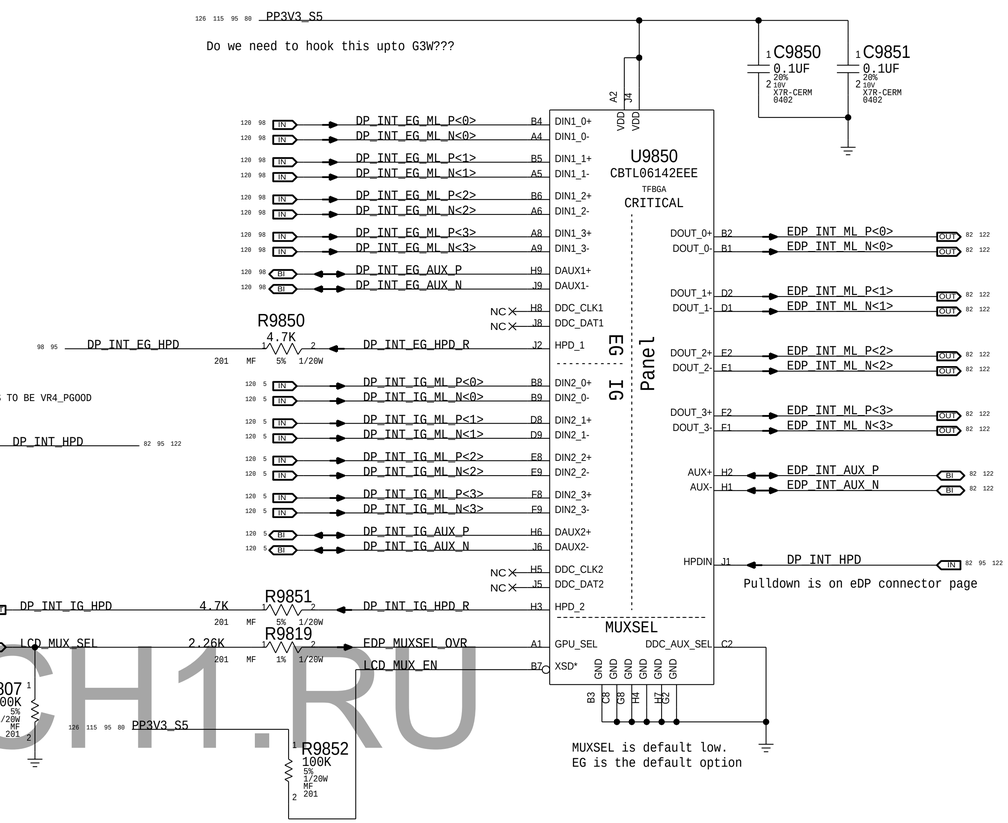

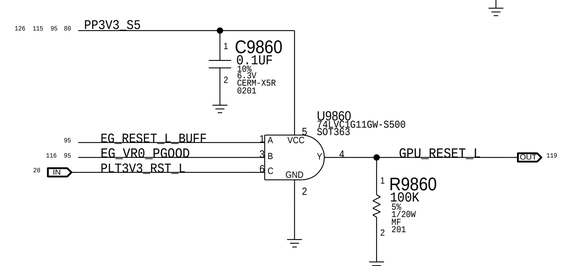

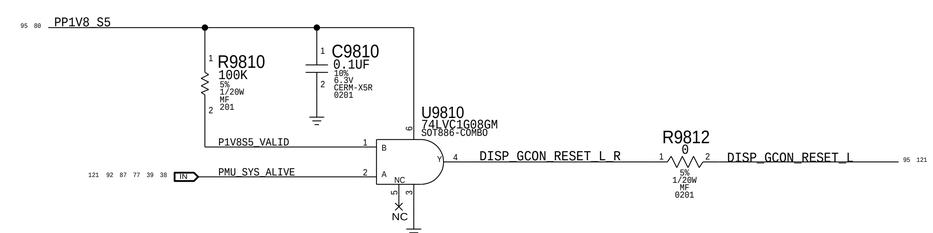

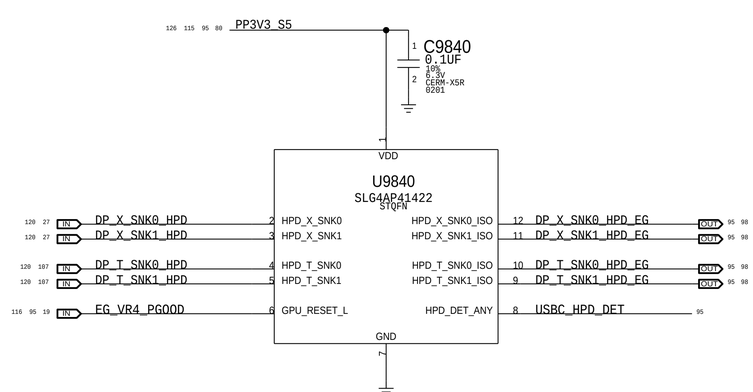

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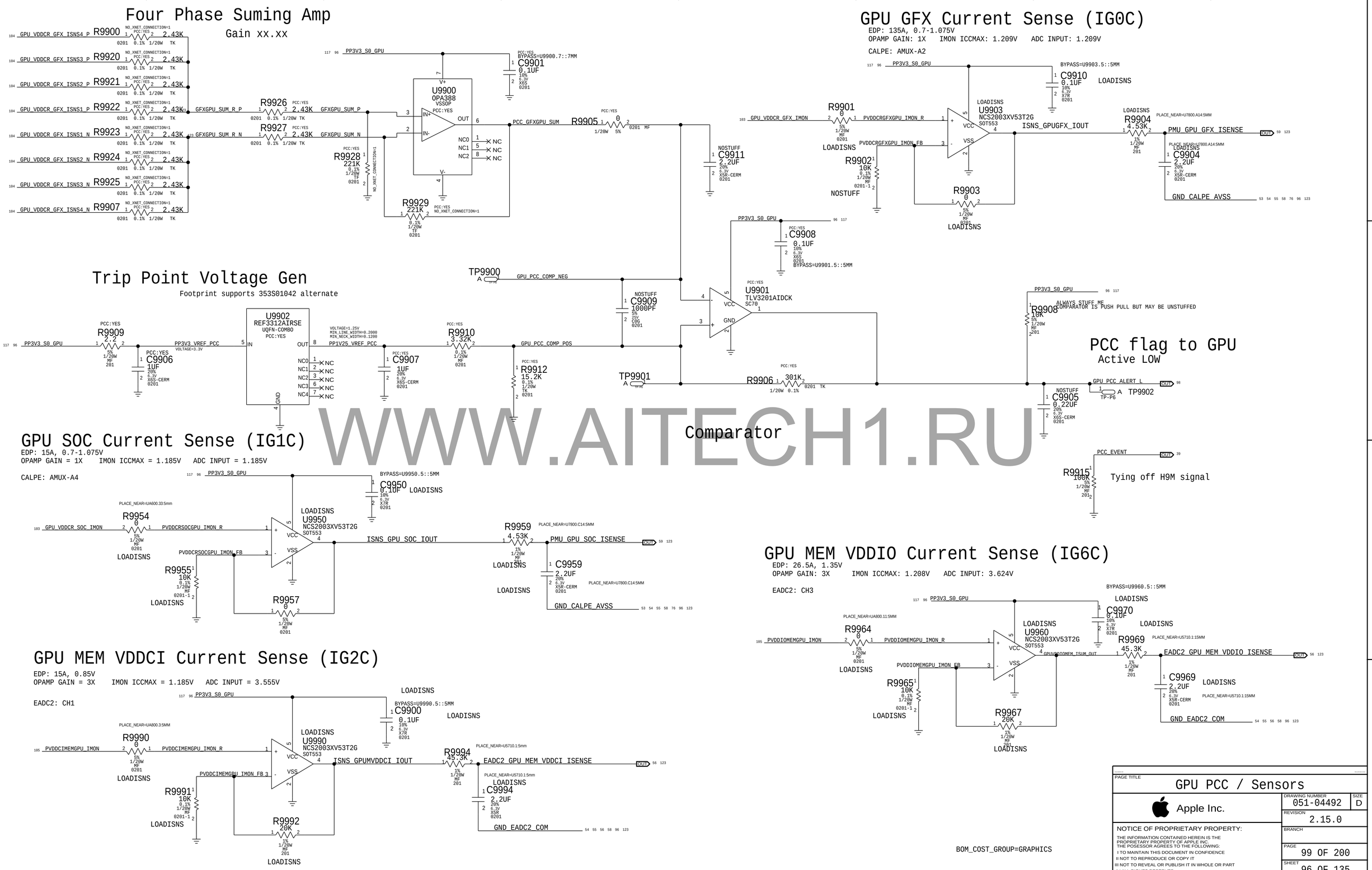

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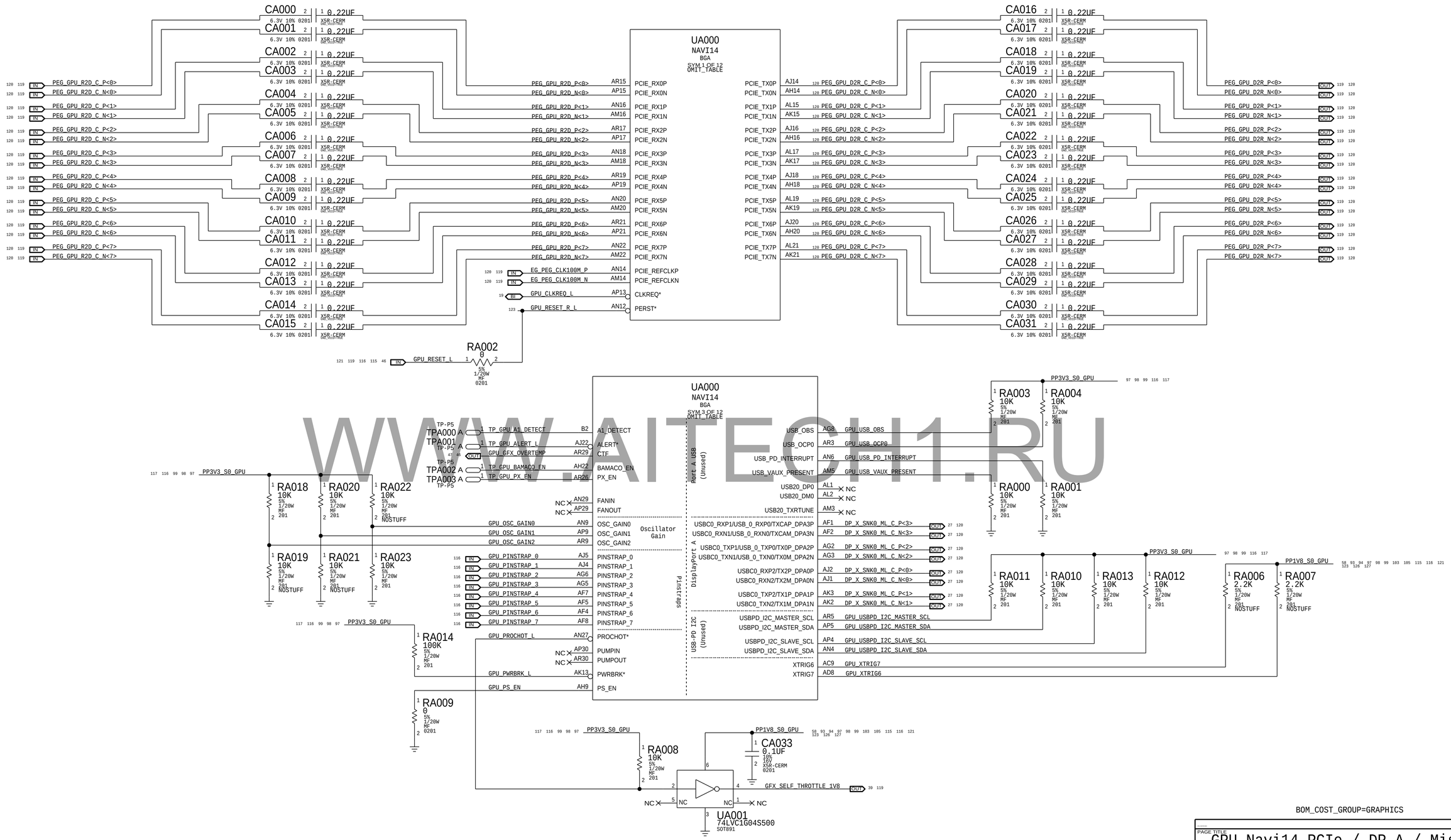

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PAGE TITLE
GPU Navi14 PCIe / DP A / Misc

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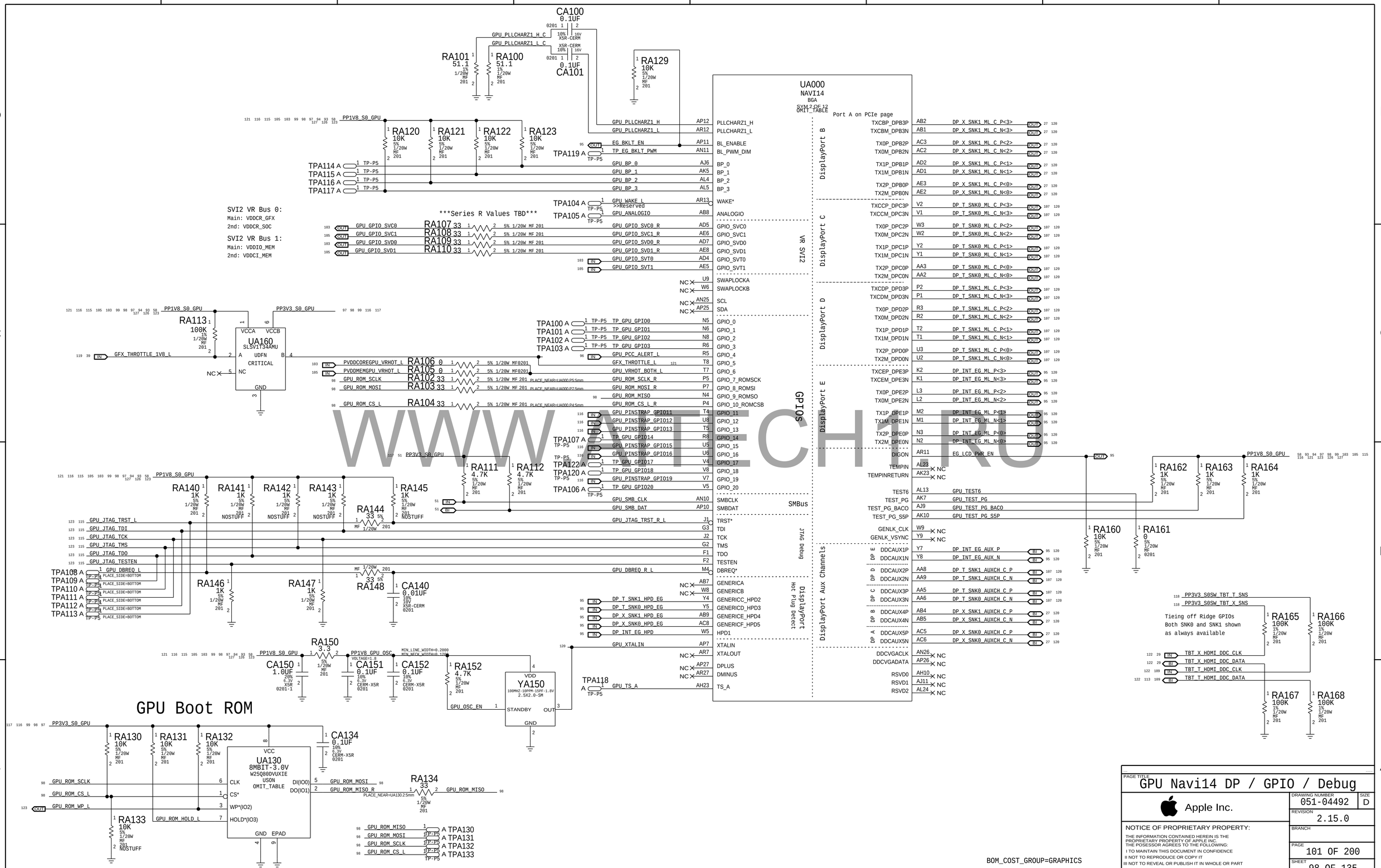

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PAGE TITLE
GPU Navi14 DP / GPIO / Debug

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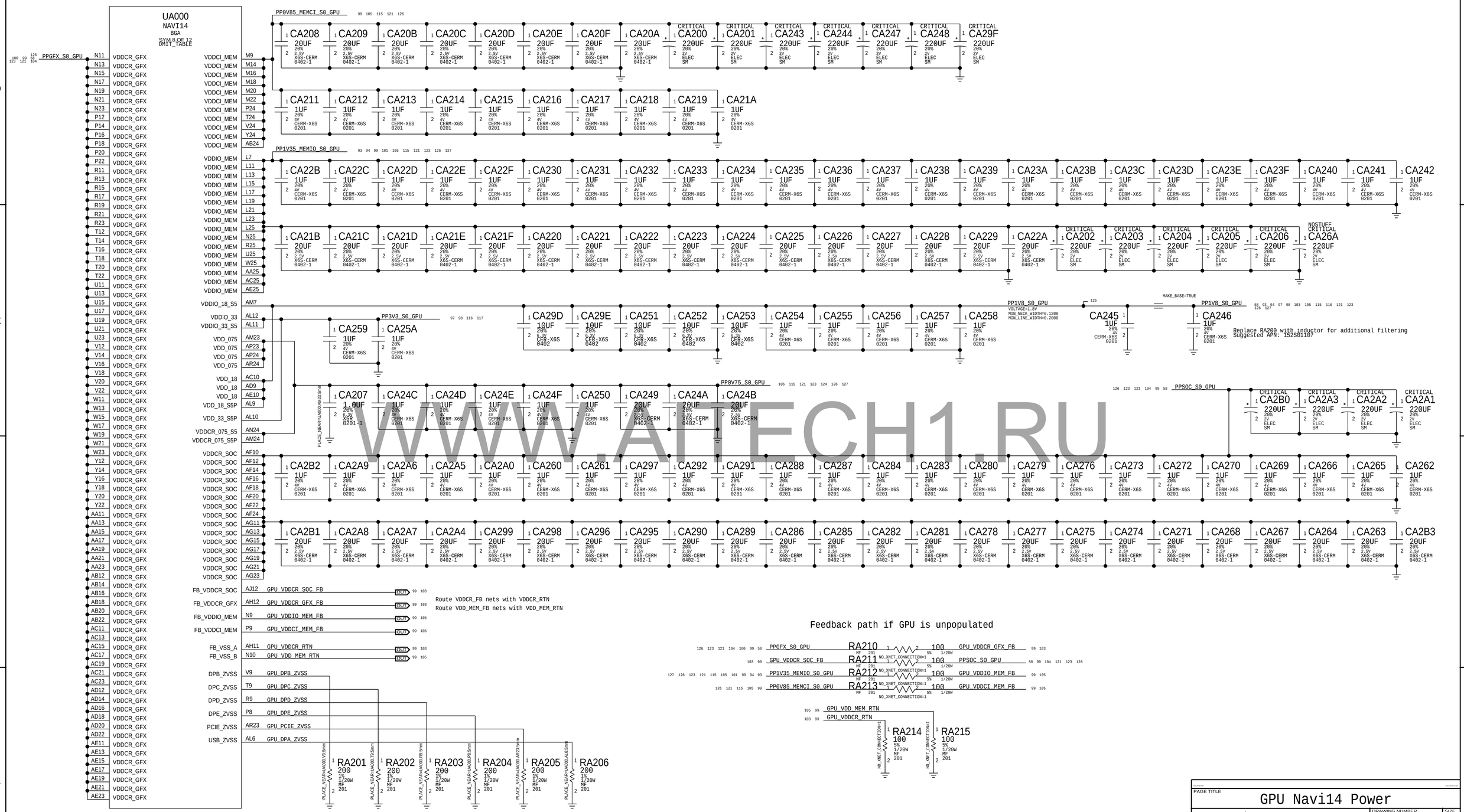

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PAGE TITLE
GPU Navi14 Power

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220UF 20% 2V ELEC SM

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A7 VSS	VSS E10	J18 VSS	VSS P23
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AA24 VSS	VSS AE24	AK14 VSS	VSS AR14
AA28 VSS	VSS AE28	AK16 VSS	VSS AR16
AA30 VSS	VSS AE30	AK18 VSS	VSS AR18
AA32 VSS	VSS AE32	AK20 VSS	VSS AR20
AA34 VSS	VSS AE34	AK22 VSS	VSS AR22
AB3 VSS	VSS AF3	AK26 VSS	VSS AR25
AB6 VSS	VSS AF6	AK30 VSS	VSS AR34
AB10 VSS	VSS AF11	AK32 VSS	
AB11 VSS	VSS AF13	AK34 VSS	
AB13 VSS	VSS AF15		

BOM_COST_GROUP=GRAPHICS

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PAGE TITLE: GPU Navi14 VSS & Decoupling

Apple Inc.

DRAWING NUMBER: 051-04492 SIZE: D

REVISION: 2.15.0

BRANCH:

PAGE: 103 OF 200

SHEET: 100 OF 135

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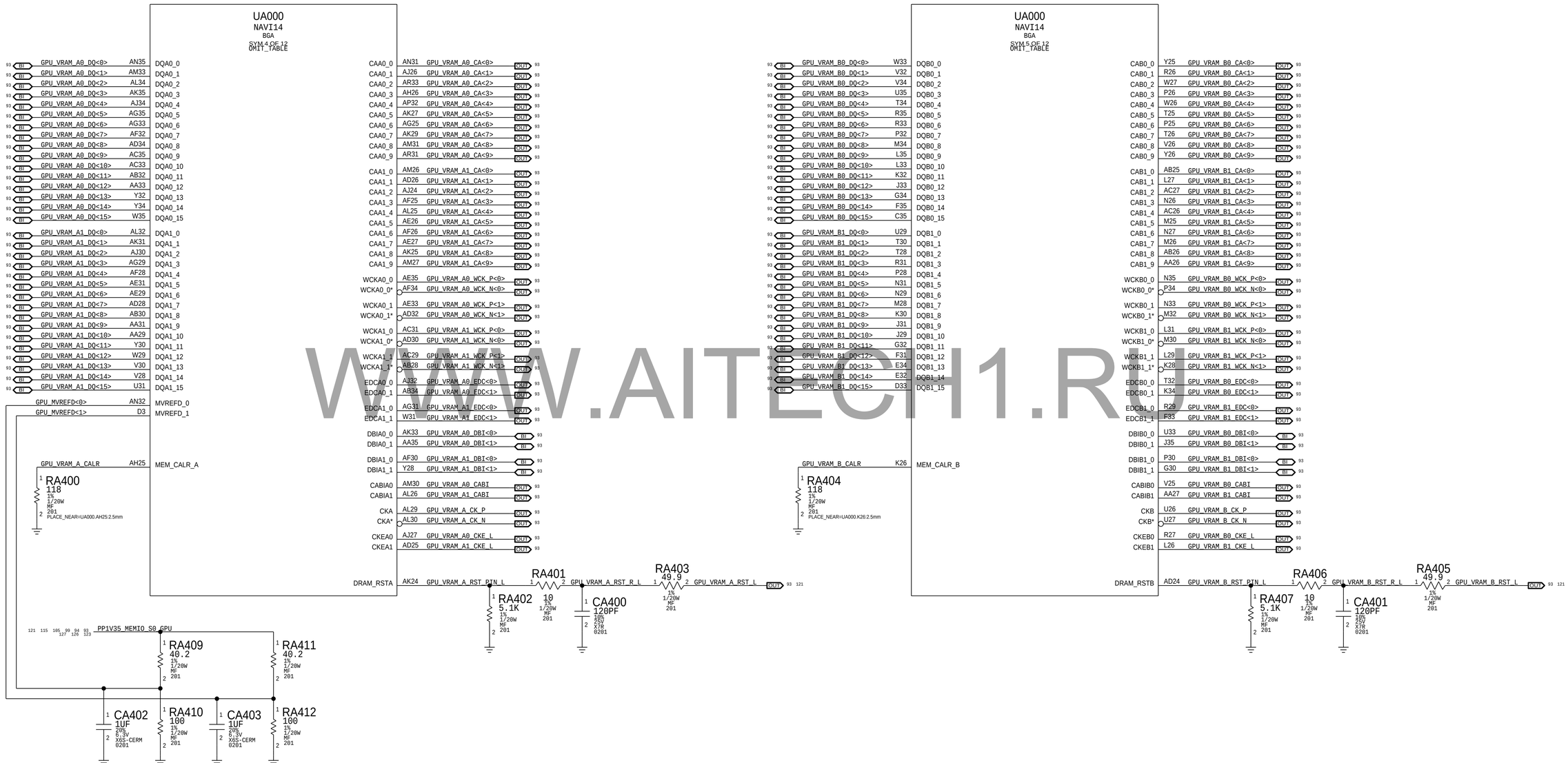

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PAGE TITLE
GPU Navi14 GDDR6 CHs A, B

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DRAWING NUMBER 051-04492 SIZE D

REVISION 2.15.0

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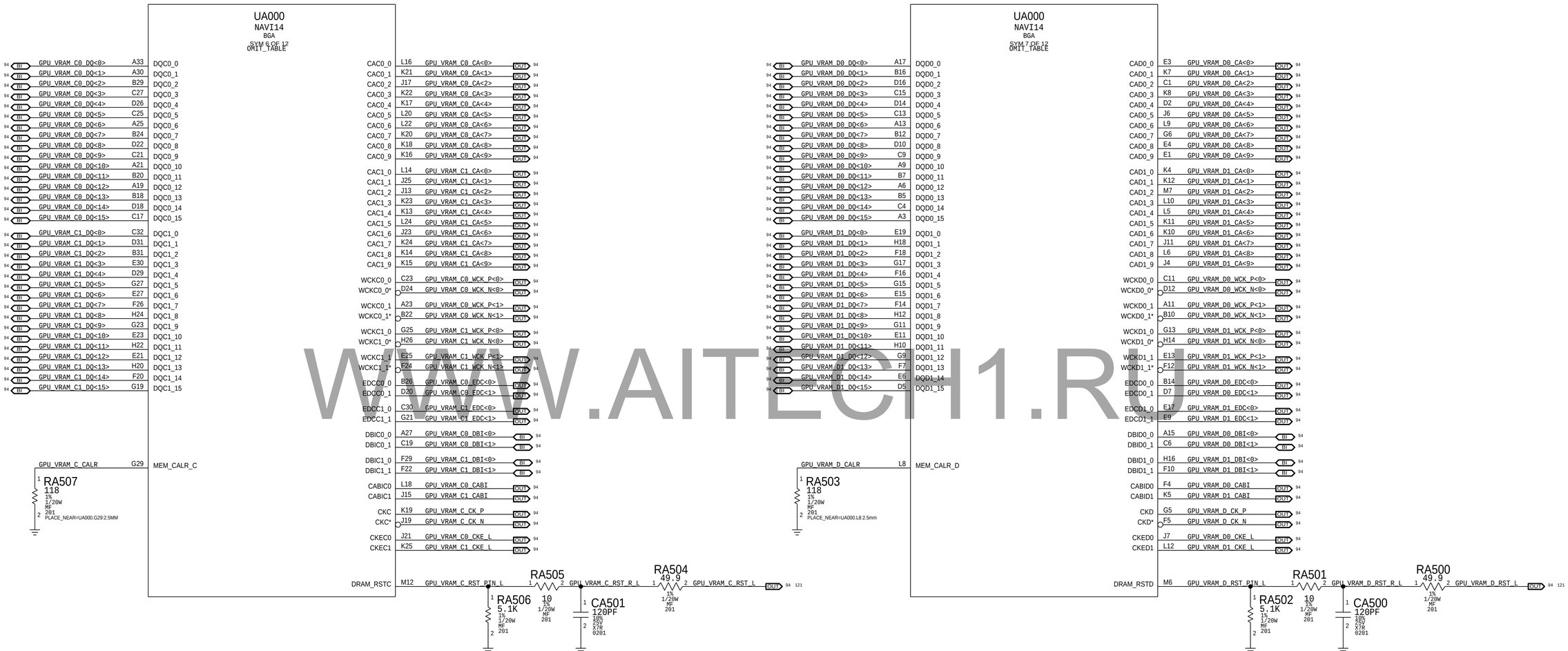

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PAGE TITLE
GPU Navi14 GDDR6 CHs C, D

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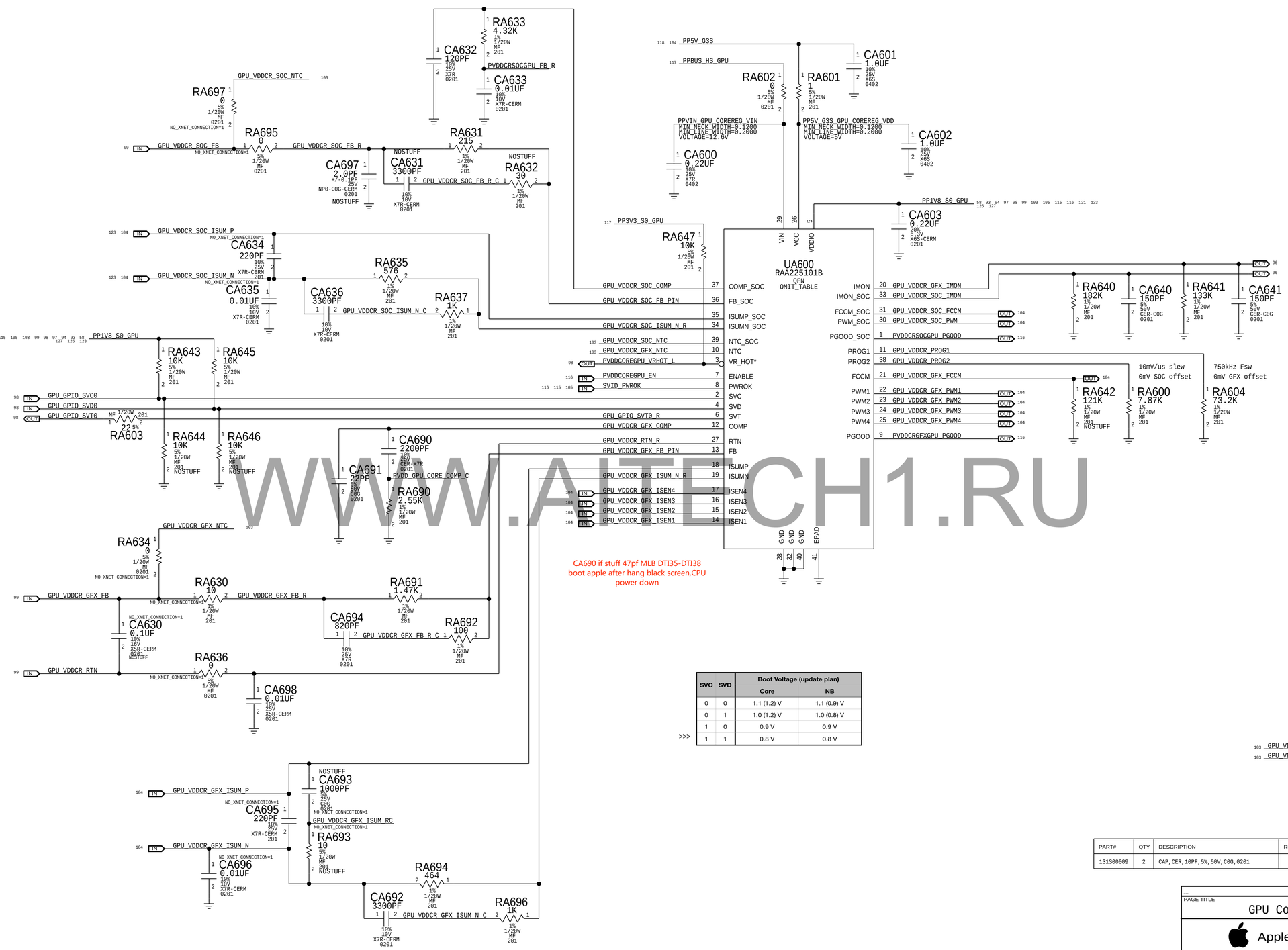
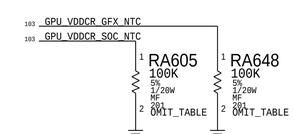


SVC	SVD	Boot Voltage (update plan)	
		Core	NB
0	0	1.1 (1.2) V	1.1 (0.9) V
0	1	1.0 (1.2) V	1.0 (0.8) V
1	0	0.9 V	0.9 V
1	1	0.8 V	0.8 V



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
131S00009	2	CAP,CER,10PF,5%,50V,C0G,0201	RA605,RA648	

BOM_COST_GROUP=GRAPHICS

PAGE TITLE
GPU Core Rails Controller

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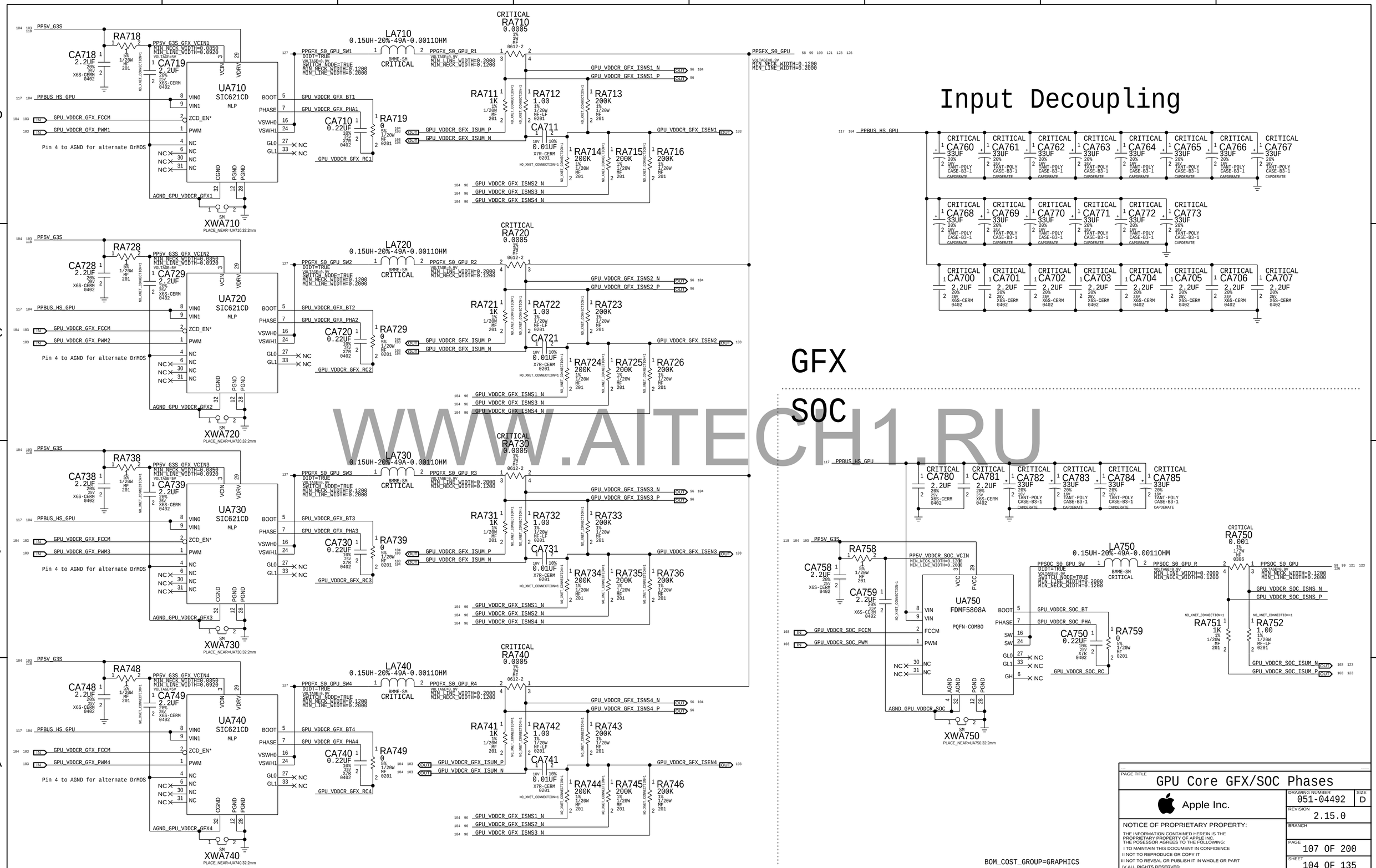

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PAGE TITLE: GPU Core GFX/SOC Phases

Apple Inc.

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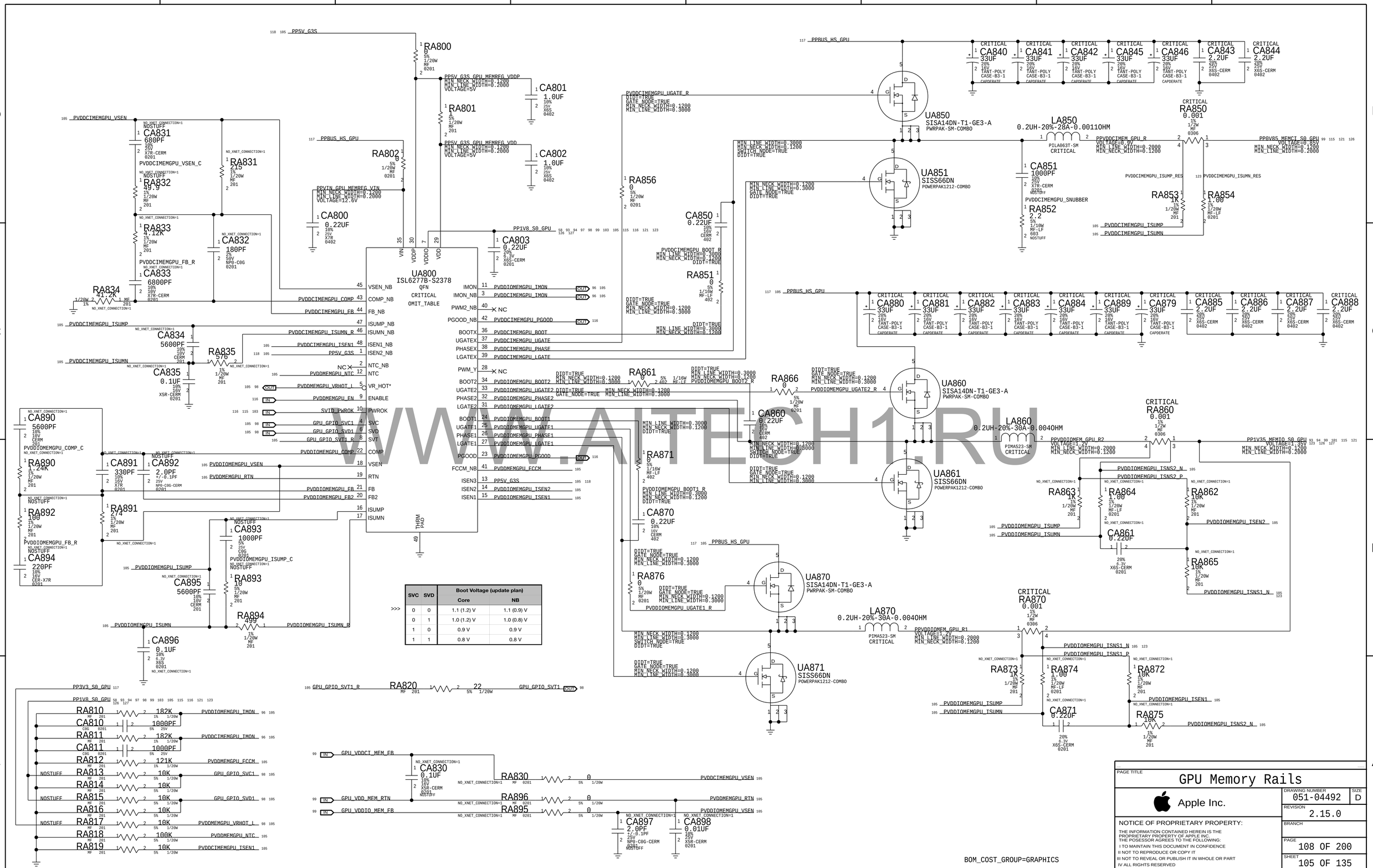

SVC	SVD	Boot Voltage (update plan) Core	Boot Voltage (update plan) NB
0	0	1.1 (1.2) V	1.1 (0.9) V
0	1	1.0 (1.2) V	1.0 (0.8) V
1	0	0.9 V	0.9 V
1	1	0.8 V	0.8 V

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PAGE TITLE: GPU Memory Rails

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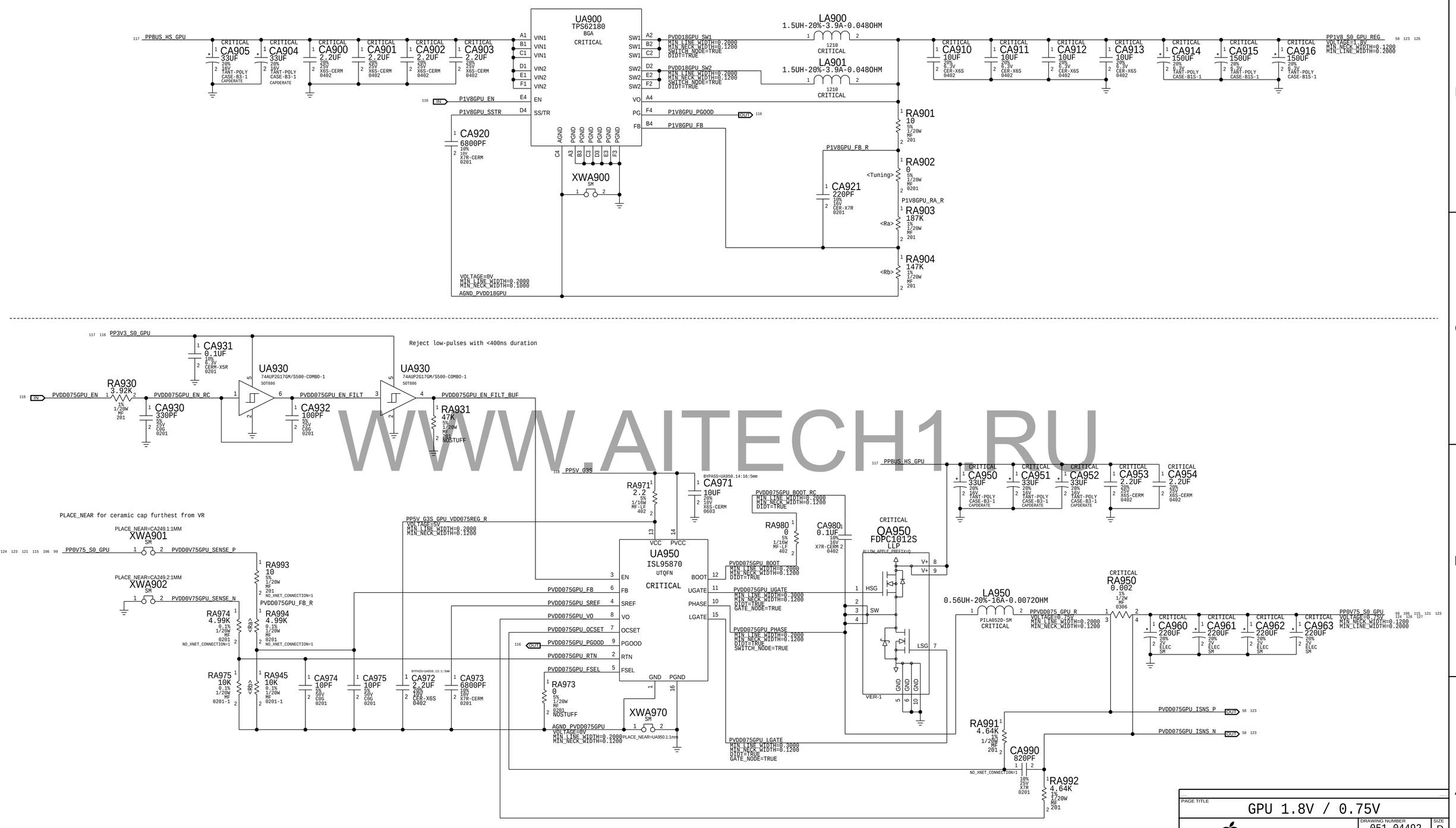

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PAGE TITLE	GPU 1.8V / 0.75V
Apple Inc.	DRAWING NUMBER 051-04492 · SIZE D
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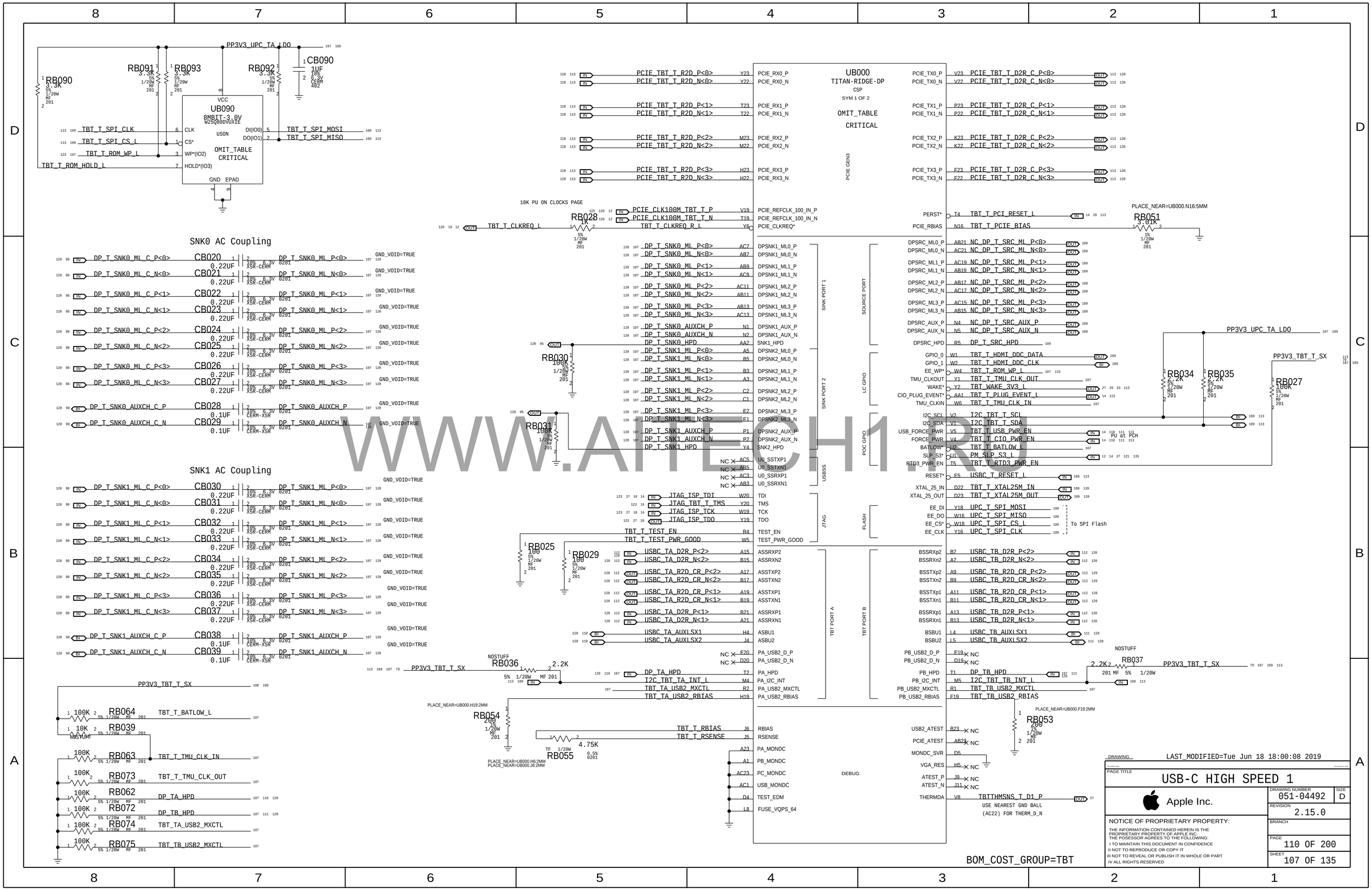

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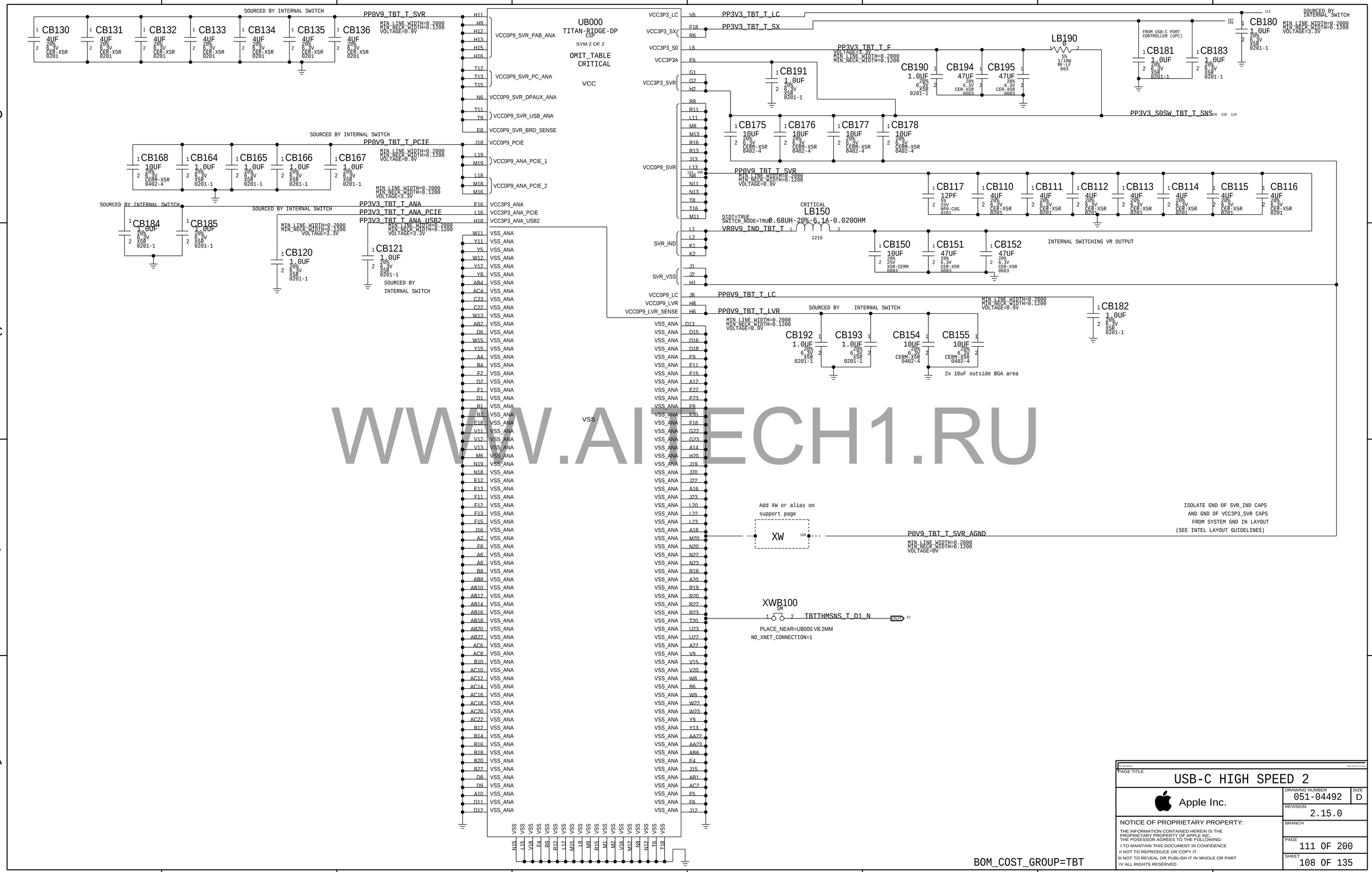

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PAGE TITLE
USB-C HIGH SPEED 2

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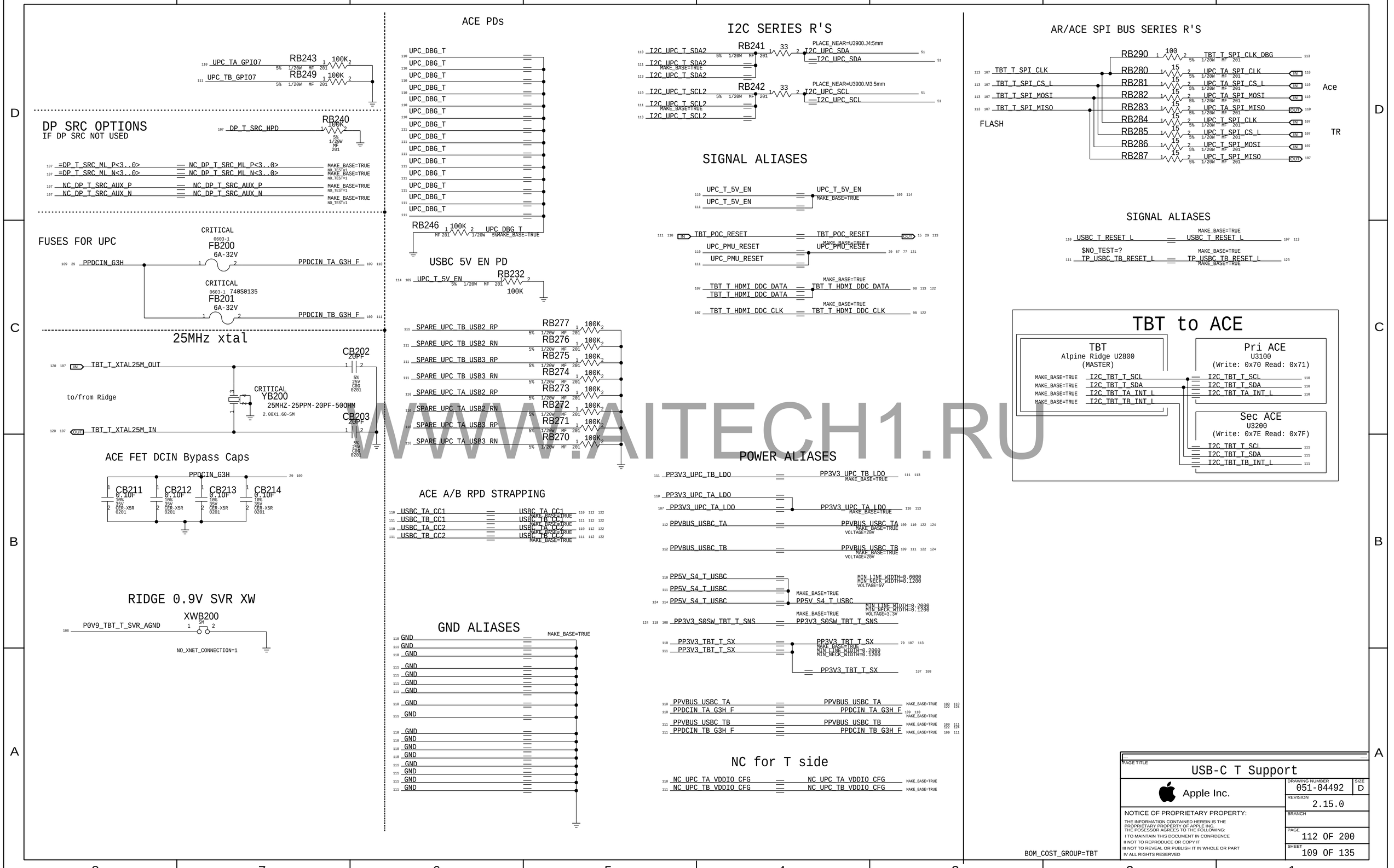

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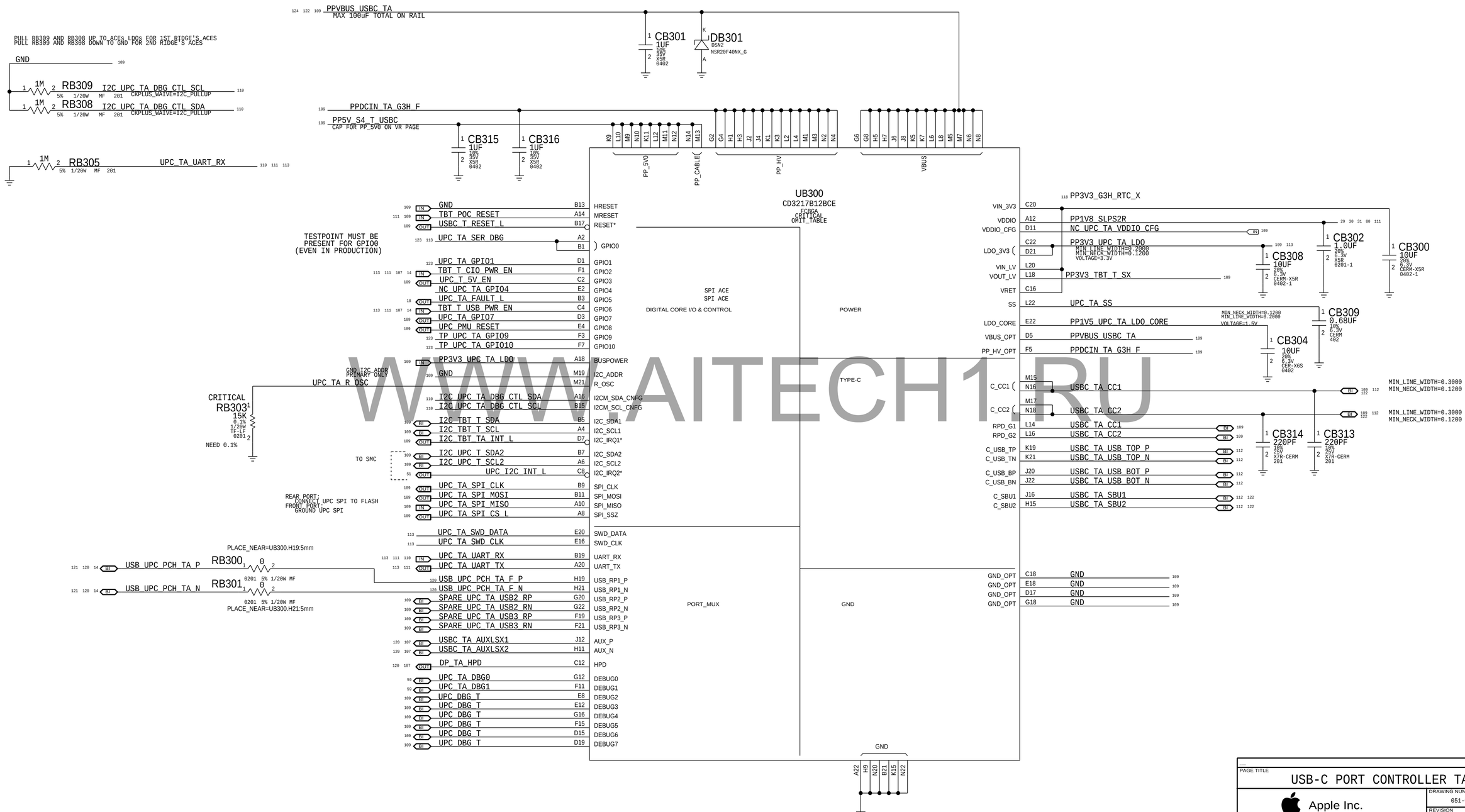
PRIMARY ACE USB-C PORT CONTROLLER (UPC)



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PAGE TITLE: USB-C PORT CONTROLLER TA

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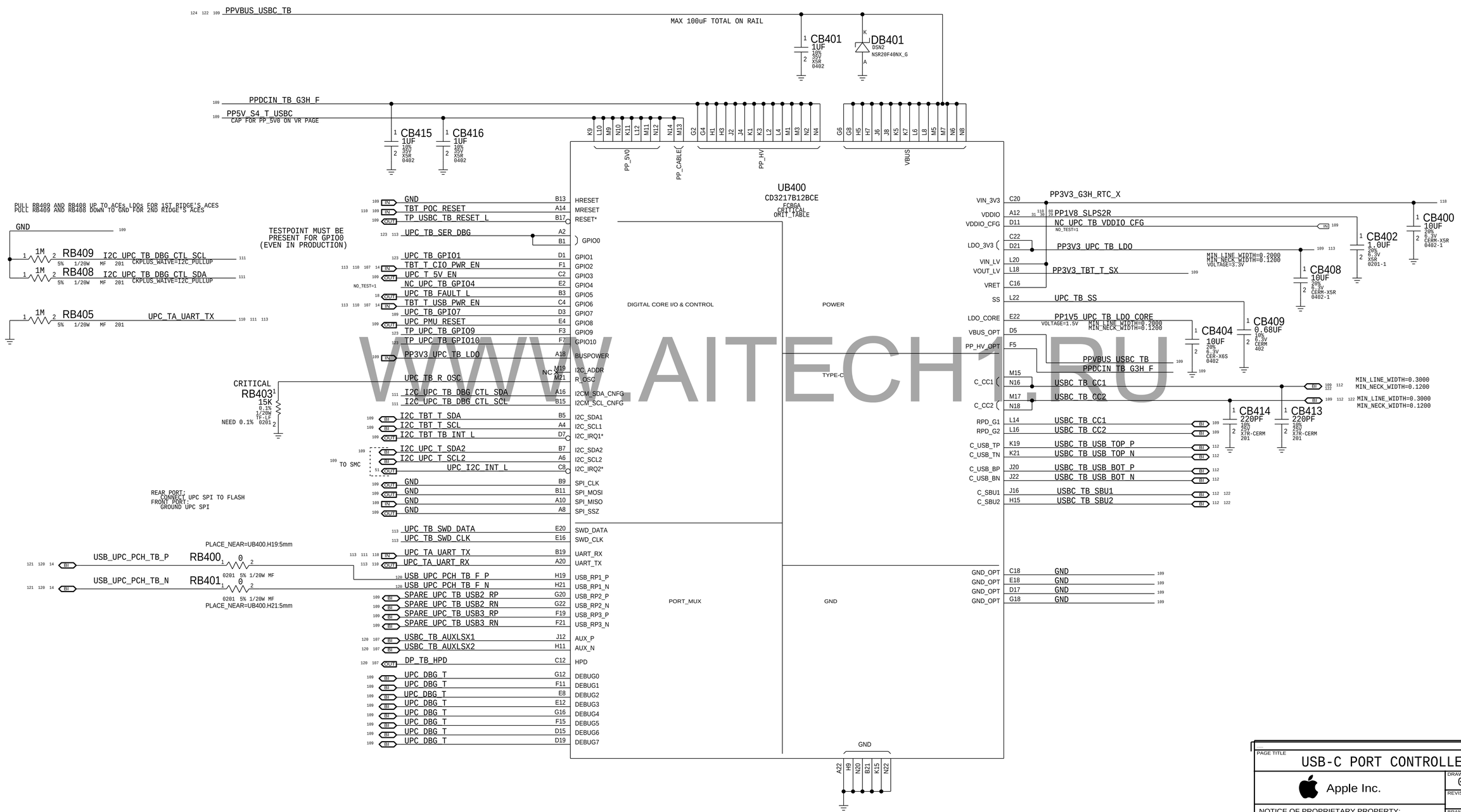
SECONDARY ACE USB-C PORT CONTROLLER (UPC)



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PAGE TITLE	USB-C PORT CONTROLLER TB
Apple Inc.	DRAWING NUMBER 051-04492 SIZE D
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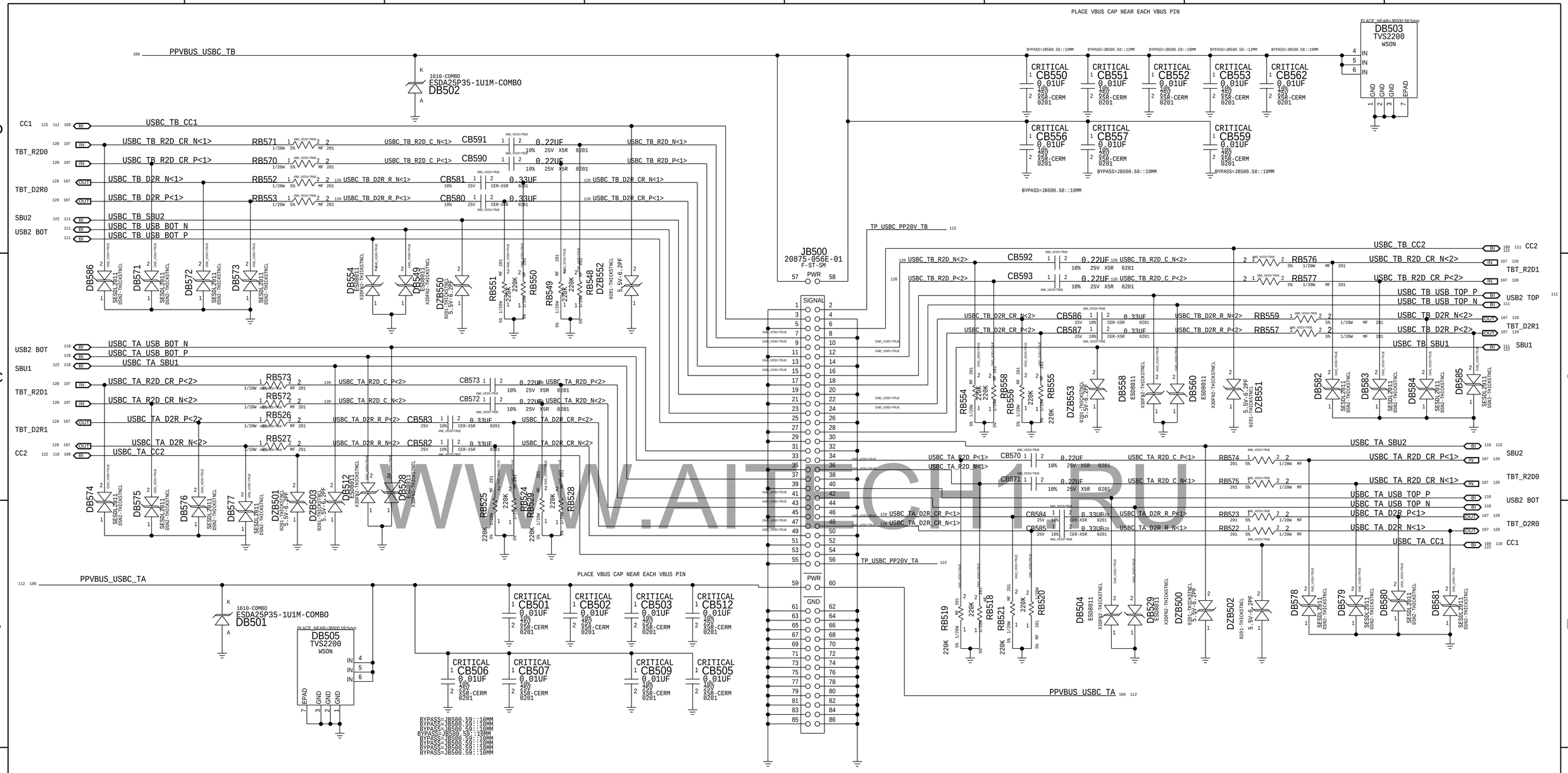

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LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE
USB-C T CONNECTOR

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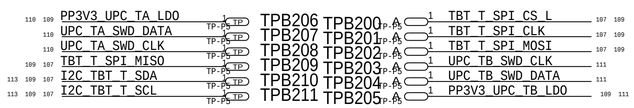
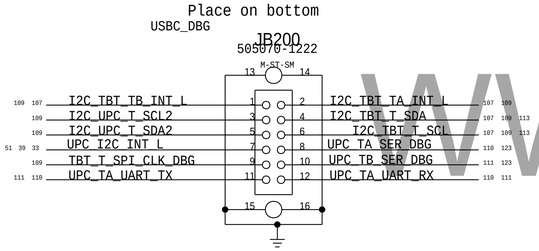
AARDVARKANOID CONN



ACE ARKANOID CONN

Place on bottom



RIDGE ARKANOID CONN

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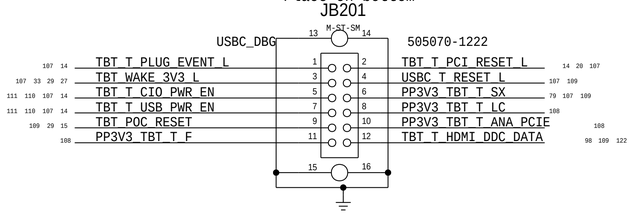
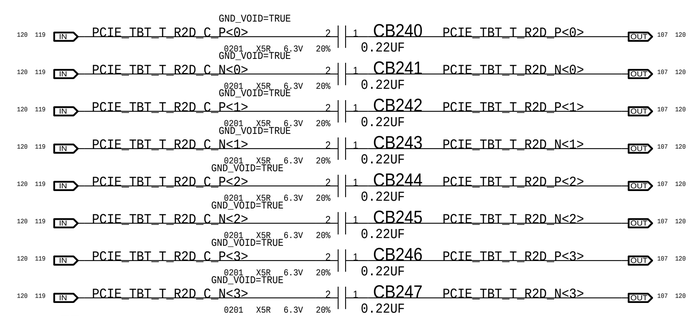
JB201

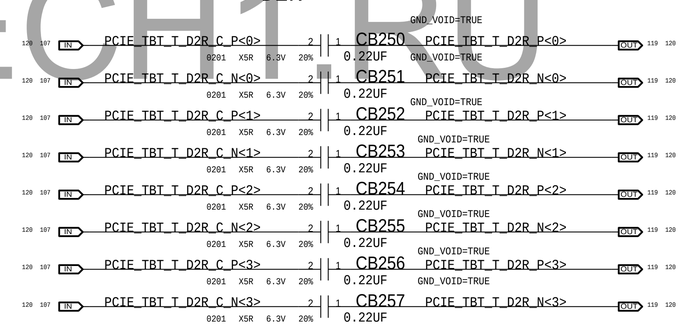


Ridge PCIE Caps

R2D



D2R



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BOM_COST_GROUP=USB-C

DESIGN: X1032/MLB_P4BP
LAST CHANGE: Fri Jan 6 16:01:21 2017

PAGE TITLE
USBC T Connector Support

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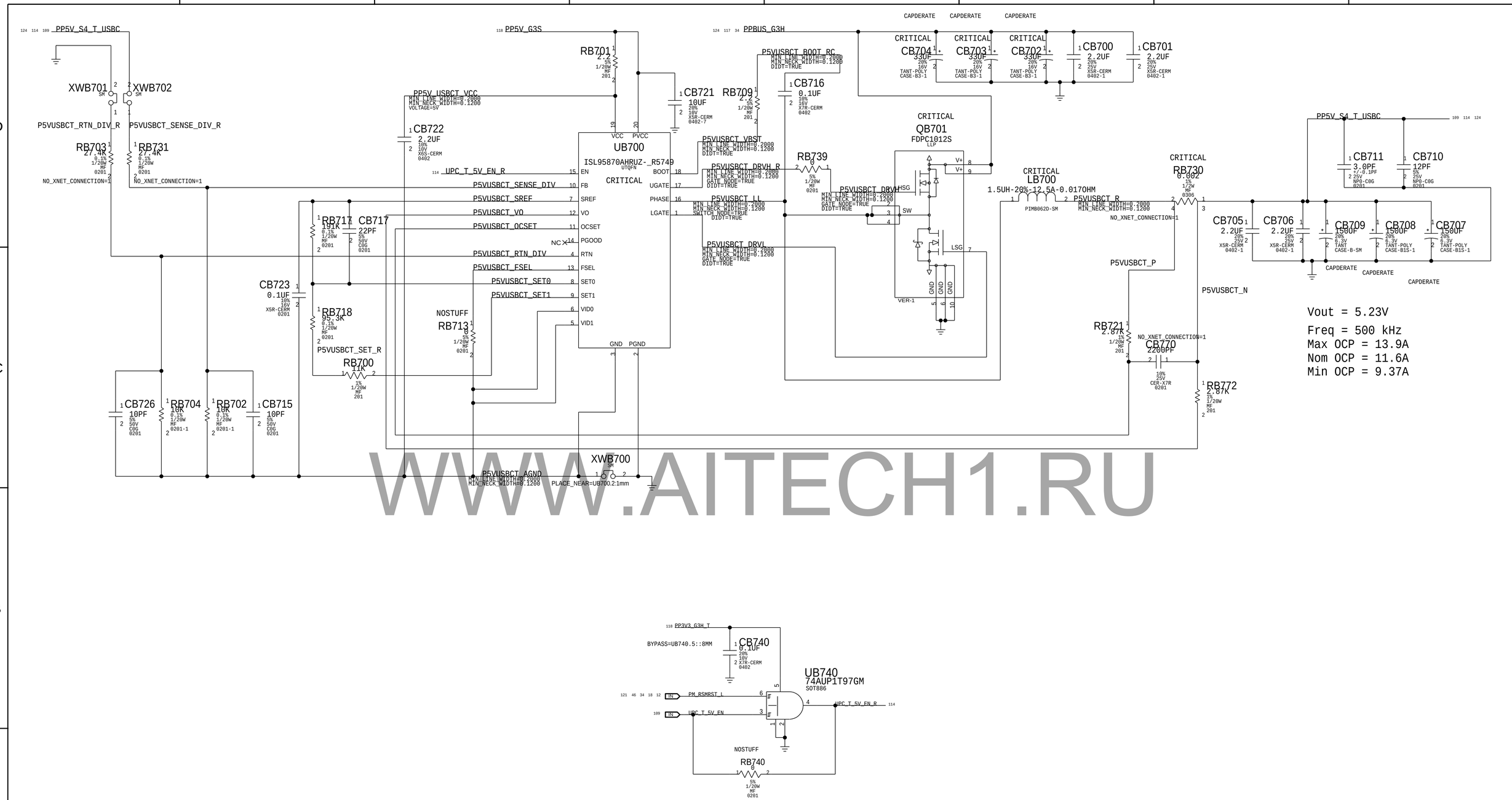

BOM_COST_GROUP=USB-C

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PAGE TITLE: USB-C T 5V VR

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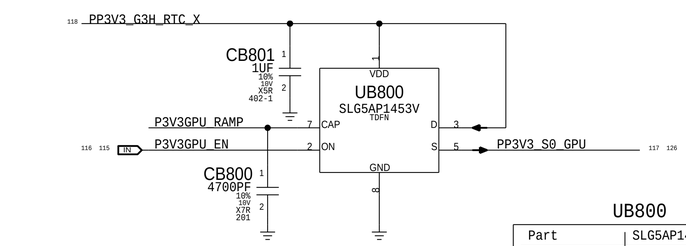
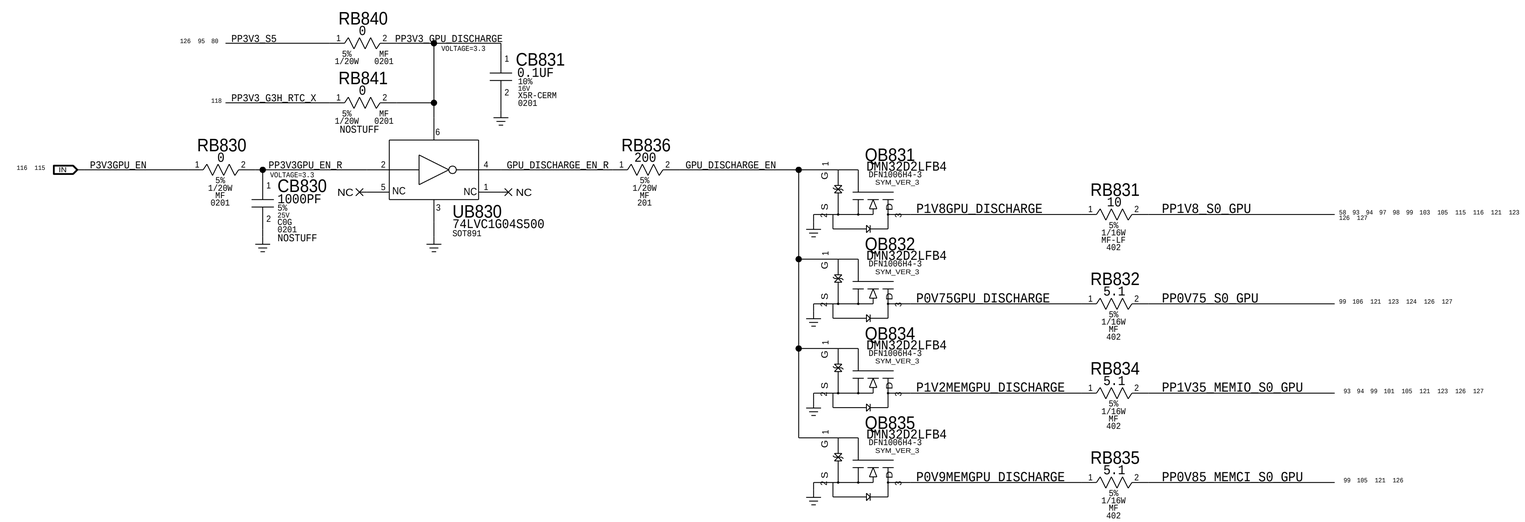


UB800

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max
T(total-on)	1.5ms

Active Discharge



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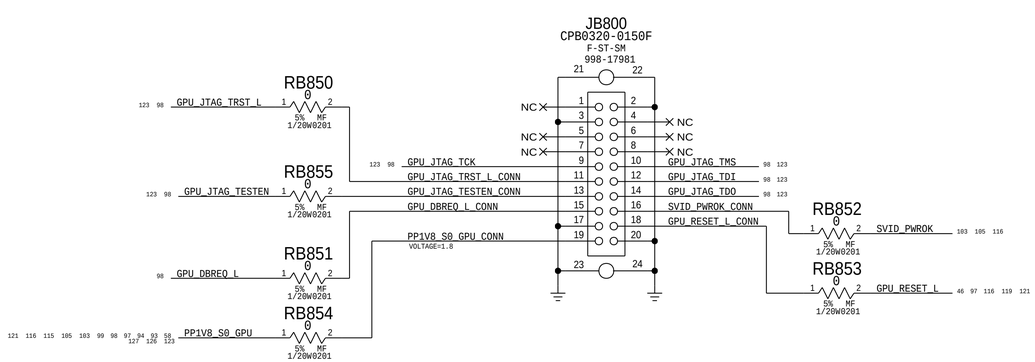
Nano-HDT



BOM_COST_GROUP=GRAPHICS

PAGE TITLE
GPU 3.3V / Discharge

Apple Inc.

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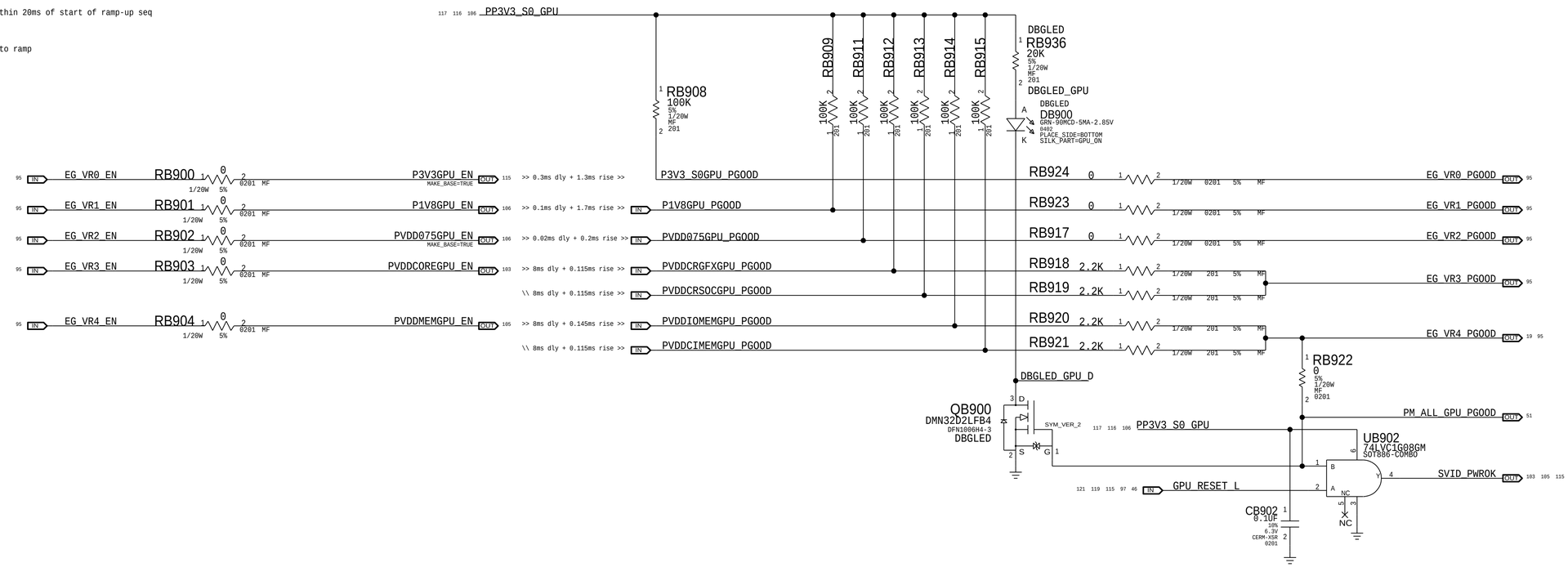
AMD POWER SEQUENCE REQUIREMENTS:

>> All GPU supplies (except VDDIO_33) must reach their nominal voltages within 20ms of start of ramp-up seq
(Shorter duration is preferred)
>> VDDIO_33 is recommended to ramp first
>> VDD_18 must reach steaty state >10us before VDDCR_x and VDDx_MEM start to ramp
>> GDDR6 VPP should reach its nominal voltage before applying VDDIO_MEM
>> PERSTB must wait >100ms to de-assert after all rails are stable
>> PCIE_REFCLK must be stable >100us before PERSTB de-assert
>> All rails (except VDDIO_33) must ramp-down within 20ms

GCON POWER SEQUENCE GUIDANCE (absolute timing):

>> VR0_EN @ t=0ms
>> VR1_EN @ t=2ms
>> VR2_EN @ t=5ms
>> VR3_EN @ t=5ms
>> VR4_EN @ t=6ms



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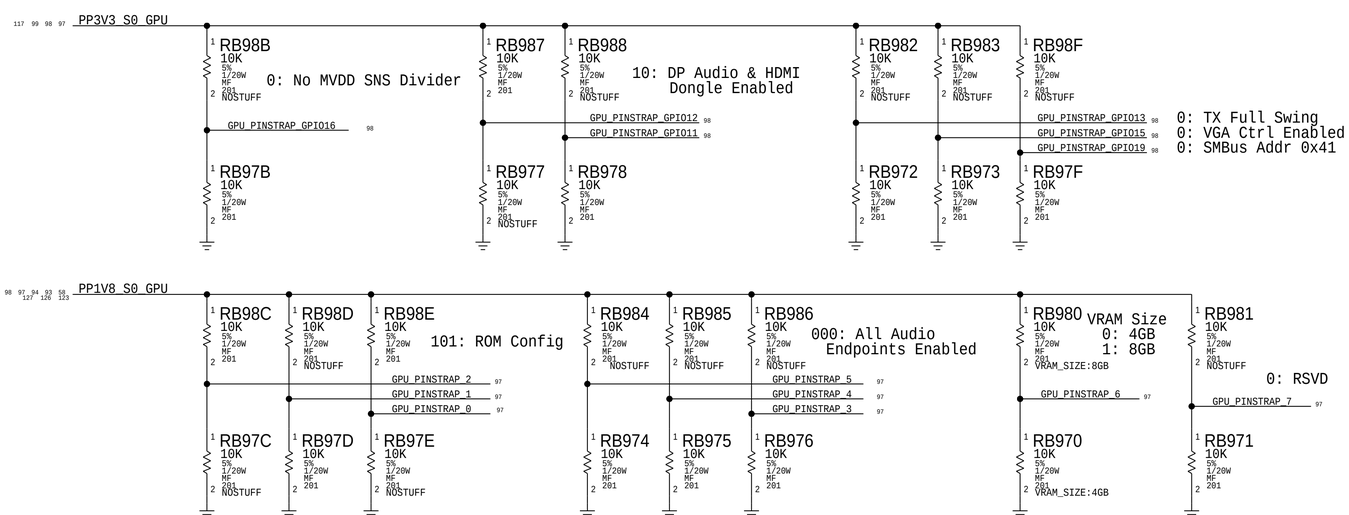

BOM_COST_GROUP=GRAPHICS

PAGE TITLE
GPU Sequencing & Straps

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PBUS & High Side

124 68 PPBUS_G3H — PPBUS_G3H — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE — 121 122 124
- PPBUS_G3H — 53
- PPBUS_G3H — 53
- PPBUS_G3H — 53
- PPBUS_G3H — 53
- PPBUS_G3H — 58
- PPBUS_G3H — 53
- PPBUS_G3H — 34 114 124
- PPBUS_G3H — 66
- PPBUS_G3H — 62 63
- PPBUS_G3H — 77
- PPBUS_G3H — 55
- PPBUS_G3H — 55
- PPBUS_G3H — 81
- PPBUS_G3H — 47

53 PPBUS_HS_CPU — PPBUS_HS_CPU — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE — 123 124 126
- PPBUS_HS_CPU — 70
- PPBUS_HS_CPU — 71
- PPBUS_HS_CPU — 72
- PPBUS_HS_CPU — 74
- PPBUS_HS_CPU — 78
- PPBUS_HS_CPU — 74
- PPBUS_HS_CPU — 69

58 PPBUS_HS_GPU — PPBUS_HS_GPU — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE — 121 123 126
- PPBUS_HS_GPU — 105
- PPBUS_HS_GPU — 105
- PPBUS_HS_GPU — 105
- PPBUS_HS_GPU — 103
- PPBUS_HS_GPU — 104
- PPBUS_HS_GPU — 104
- PPBUS_HS_GPU — 106
- PPBUS_HS_GPU — 106

53 PPBUS_HS_OTH5V — PPBUS_HS_OTH5V — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE — 123
- PPBUS_HS_OTH5V — 73

53 PPBUS_HS_3V3G3H_T — PPBUS_HS_3V3G3H_T — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE
- PPBUS_HS_3V3G3H_T — 73

53 PPBUS_HS_3V3G3HRTC_X — PPBUS_HS_3V3G3HRTC_X — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE
- PPBUS_HS_3V3G3HRTC_X — 67

CPU Rails

70 PPVCC_S0_CPU — PPVCC_S0_CPU — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.92V, MAKE_BASE=TRUE — 121 123
- PPVCC_S0_CPU
- PPVCC_S0_CPU — 6 8 58
- 10 126

71 PPVCCSA_S0_CPU — PPVCCSA_S0_CPU — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.92V, MAKE_BASE=TRUE — 121 123
- PPVCCSA_S0_CPU
- PPVCCSA_S0_CPU — 8 58 126
- 11

72 PPVCCGT_S0_CPU — PPVCCGT_S0_CPU — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.92V, MAKE_BASE=TRUE — 121 123
- PPVCCGT_S0_CPU
- PPVCCGT_S0_CPU — 8 58
- 11 124 126

124 78 PPVCCIO_S0_CPU — PPVCCIO_S0_CPU — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=0.95V, MAKE_BASE=TRUE — 121 123
- PPVCCIO_S0_CPU — 5 8 10 124

DDR4 1.2V

74 PP1V2_S3 — PP1V2_S3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.2V, MAKE_BASE=TRUE — 121 123 124 125
- PP1V2_S3
- PP1V2_S3 — 24 25
- PP1V2_S3 — 21
- PP1V2_S3 — 22 23 26
- PP1V2_S3 — 54
- PP1V2_S3 — 79

54 PP1V2_S3_CPUDDR — PP1V2_S3_CPUDDR — MIN_NECK_WIDTH=0.1200, MIN_LINE_WIDTH=0.2000, MAKE_BASE=TRUE, VOLTAGE=1.2V — 122 123
- PP1V2_S3_CPUDDR — 8
- PP1V2_S3_CPUDDR — 10 124 125

79 PP1V2_S0SW — PP1V2_S0SW — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.2V, MAKE_BASE=TRUE — 121
- PP1V2_S0SW — 8

21 PP0V6_S3_MEM_VREFCA_A — PP0V6_S3_MEM_VREFCA_A — MAKE_BASE=TRUE, VOLTAGE=0.6V — 22 23

21 PP0V6_S3_MEM_VREFCA_B — PP0V6_S3_MEM_VREFCA_B — MAKE_BASE=TRUE, VOLTAGE=0.6V — 24 25

DDR4 0.6V VTT

74 PP0V6_S0_DDRVTT — PP0V6_S0_DDRVTT — MIN_LINE_WIDTH=0.4000, MIN_NECK_WIDTH=0.1200, VOLTAGE=0.6V, MAKE_BASE=TRUE — 122
- PP0V6_S0_DDRVTT — 124
- PP0V6_S0_DDRVTT — 124
- PP0V6_S0_DDRVTT — 26
- PP0V6_S0_DDRVTT — 26

DDR4 2.5V

74 PP2V5_S3 — PP2V5_S3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=2.5V, MAKE_BASE=TRUE — 121 124 125
- PP2V5_S3 — 22 23
- PP2V5_S3 — 24 25
- PP2V5_S3 — 74

PMIC Buck 8 - PCH 1.05V Prime

54 PP1V05_PRIM — PP1V05_PRIM — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.05V, MAKE_BASE=TRUE — 121 123
- PP1V05_PRIM — 16 17 80
- PP1V05_PRIM — 17
- PP1V05_PRIM — 16
- PP1V05_PRIM — 16
- PP1V05_PRIM — 16
- PP1V05_PRIM — 17
- PP1V05_PRIM — 16 17
- PP1V05_PRIM — 17
- PP1V05_PRIM — 18
- PP1V05_PRIM — 74

PMIC Buck8 SW2

75 PP1V05_S3 — PP1V05_S3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.05V, MAKE_BASE=TRUE — 121
- PP1V05_S3 — 6 8 11 46
- PP1V05_S3 — 69
- PP1V05_S3 — 8 11
- PP1V05_S3 — 46
- PP1V05_S3 — 77

PMIC HIO SW

76 PP1V05_S0SW — PP1V05_S0SW — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.05V, MAKE_BASE=TRUE — 121
- PP1V05_S0SW — 6 8 11
- PP1V05_S0SW — 18

GPU Rails

126 115 PP3V3_S0_GPU — PP3V3_S0_GPU — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=3.3V, MAKE_BASE=TRUE — 121
- PP3V3_S0_GPU — 97 98 99 116
- PP3V3_S0_GPU — 19
- PP3V3_S0_GPU — 51 98
- PP3V3_S0_GPU — 96
- PP3V3_S0_GPU — 105
- PP3V3_S0_GPU — 103
- PP3V3_S0_GPU — 106 116

Digital Ground

GND — MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000

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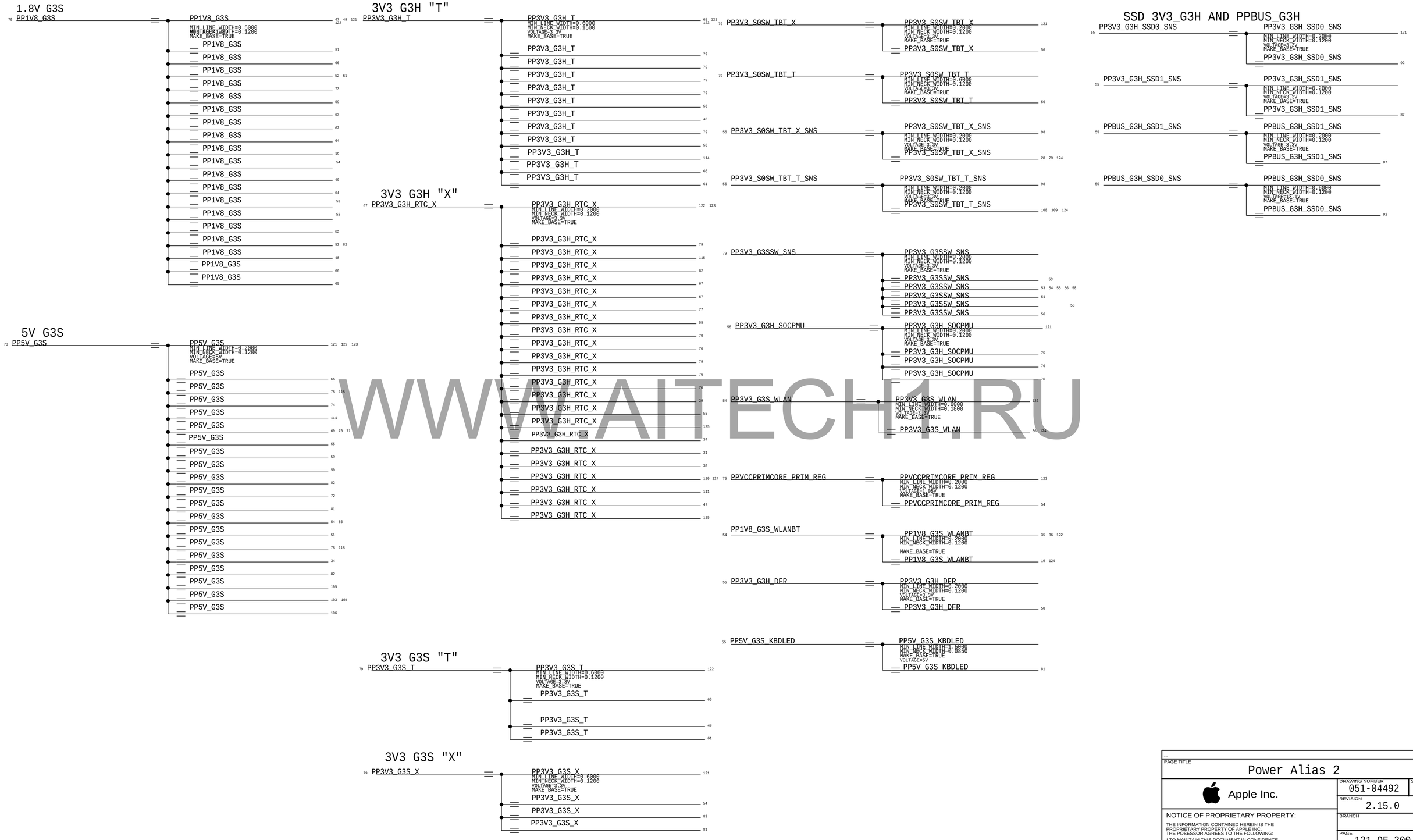

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PEG X16 CPU-GPU

PEG_GPU_D2R_P<7..0> (IN, MAKE_BASE=TRUE)	=	=PEG_D2R_P<7..0>	(OUT)
PEG_GPU_D2R_N<7..0> (IN, MAKE_BASE=TRUE)	=	=PEG_D2R_N<7..0>	(OUT)
PEG_GPU_R2D_C_P<7..0> (OUT, MAKE_BASE=TRUE)	=	=PEG_R2D_C_P<7..0>	(IN)
PEG_GPU_R2D_C_N<7..0> (OUT, MAKE_BASE=TRUE)	=	=PEG_R2D_C_N<7..0>	(IN)

CPU Display Aliases

NC_DDI1_ML_C_P<3..0> (MAKE_BASE=TRUE, NO_TEST=1)	=	NC_DDI1_ML_C_P<3..0>	(IN)
NC_DDI1_ML_C_N<3..0> (MAKE_BASE=TRUE, NO_TEST=1)	=	NC_DDI1_ML_C_N<3..0>	(IN)
NC_DDI1_AUXCH_C_P (MAKE_BASE=TRUE)	=	NC_DDI1_AUXCH_C_P	(IN)
NC_DDI1_AUXCH_C_N (MAKE_BASE=TRUE)	=	NC_DDI1_AUXCH_C_N	(IN)
NC_DDI2_ML_C_P<3..0> (MAKE_BASE=TRUE, NO_TEST=1)	=	NC_DDI2_ML_C_P<3..0>	(IN)
NC_DDI2_ML_C_N<3..0> (MAKE_BASE=TRUE, NO_TEST=1)	=	NC_DDI2_ML_C_N<3..0>	(IN)
NC_DDI2_AUXCH_C_P (MAKE_BASE=TRUE)	=	NC_DDI2_AUXCH_C_P	(IN)
NC_DDI2_AUXCH_C_N (MAKE_BASE=TRUE)	=	NC_DDI2_AUXCH_C_N	(IN)
NC_DDI3_ML_P<3..0> (MAKE_BASE=TRUE, NO_TEST=1)	=	NC_DDI3_ML_P<3..0>	(IN)
NC_DDI3_ML_N<3..0> (MAKE_BASE=TRUE, NO_TEST=1)	=	NC_DDI3_ML_N<3..0>	(IN)
NC_DDI3_AUXCH_P (MAKE_BASE=TRUE)	=	NC_DDI3_AUXCH_P	(IN)
NC_DDI3_AUXCH_N (MAKE_BASE=TRUE)	=	NC_DDI3_AUXCH_N	(IN)

GPU Throttle

H9M Side (After LS)		GPU Side
GFX_SELF_THROTTLE_1V8 (MAKE_BASE=TRUE)	=	GFX_SELF_THROTTLE_1V8
GFX_THROTTLE_1V8_L (MAKE_BASE=TRUE)	=	GFX_THROTTLE_1V8_L

Thunderbolt Signals Through PEG

PCIE_TBT_X_D2R_P<3..0> (IN, MAKE_BASE=TRUE)	=	=PEG_D2R_P<11..8>	(OUT)
PCIE_TBT_X_D2R_N<3..0> (IN, MAKE_BASE=TRUE)	=	=PEG_D2R_N<11..8>	(OUT)
PCIE_TBT_X_R2D_C_P<3..0> (OUT, MAKE_BASE=TRUE)	=	=PEG_R2D_C_P<11..8>	(IN)
PCIE_TBT_X_R2D_C_N<3..0> (OUT, MAKE_BASE=TRUE)	=	=PEG_R2D_C_N<11..8>	(IN)
PCIE_TBT_T_D2R_P<3..0> (IN, MAKE_BASE=TRUE)	=	=PEG_D2R_P<15..12>	(OUT)
PCIE_TBT_T_D2R_N<3..0> (IN, MAKE_BASE=TRUE)	=	=PEG_D2R_N<15..12>	(OUT)
PCIE_TBT_T_R2D_C_P<3..0> (OUT, MAKE_BASE=TRUE)	=	=PEG_R2D_C_P<15..12>	(IN)
PCIE_TBT_T_R2D_C_N<3..0> (OUT, MAKE_BASE=TRUE)	=	=PEG_R2D_C_N<15..12>	(IN)

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GPU ALIAS

GPU_RESET_L (IN)	=	GPU_RESET_L (MAKE_BASE=TRUE)	(OUT)
EG_PEG_CLK100M_N (IN, MAKE_BASE=TRUE)	=	EG_PEG_CLK100M_N	(OUT)
EG_PEG_CLK100M_P (IN, MAKE_BASE=TRUE)	=	EG_PEG_CLK100M_P	(OUT)

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ICT TESTPOINTS , High Speed NO_TEST

PEG / GPU

119 97	IN	PEG_GPU_D2R_P<7..0>	NO_TEST=1
119 97	IN	PEG_GPU_D2R_N<7..0>	NO_TEST=1
97	IN	PEG_GPU_D2R_C_P<7..0>	NO_TEST=1
97	IN	PEG_GPU_D2R_C_N<7..0>	NO_TEST=1
97	IN	PEG_GPU_R2D_P<7..0>	NO_TEST=1
97	IN	PEG_GPU_R2D_N<7..0>	NO_TEST=1
119 97	IN	PEG_GPU_R2D_C_P<7..0>	NO_TEST=1
119 97	IN	PEG_GPU_R2D_C_N<7..0>	NO_TEST=1

PEG / TR

119 33	IN	PCIE_TBT_X_D2R_P<3..0>	NO_TEST=1
119 33	IN	PCIE_TBT_X_D2R_N<3..0>	NO_TEST=1
33 27	IN	PCIE_TBT_X_D2R_C_P<3..0>	NO_TEST=1
33 27	IN	PCIE_TBT_X_D2R_C_N<3..0>	NO_TEST=1
33 27	IN	PCIE_TBT_X_R2D_P<3..0>	NO_TEST=1
33 27	IN	PCIE_TBT_X_R2D_N<3..0>	NO_TEST=1
119 33	IN	PCIE_TBT_X_R2D_C_P<3..0>	NO_TEST=1
119 33	IN	PCIE_TBT_X_R2D_C_N<3..0>	NO_TEST=1
119 113	IN	PCIE_TBT_T_D2R_P<3..0>	NO_TEST=1
119 113	IN	PCIE_TBT_T_D2R_N<3..0>	NO_TEST=1
113 107	IN	PCIE_TBT_T_D2R_C_P<3..0>	NO_TEST=1
113 107	IN	PCIE_TBT_T_D2R_C_N<3..0>	NO_TEST=1
113 107	IN	PCIE_TBT_T_R2D_P<3..0>	NO_TEST=1
113 107	IN	PCIE_TBT_T_R2D_N<3..0>	NO_TEST=1
119 113	IN	PCIE_TBT_T_R2D_C_P<3..0>	NO_TEST=1
119 113	IN	PCIE_TBT_T_R2D_C_N<3..0>	NO_TEST=1

CPU EDP

95 5	IN	DP_INT_IG_ML_N<3..0>	NO_TEST=1
95 5	IN	DP_INT_IG_ML_P<3..0>	NO_TEST=1
95 5	IN	DP_INT_IG_AUX_N	
95 5	IN	DP_INT_IG_AUX_P	

DDR

23 22 26 7	IN	MEM_A_CLK_P<1..0>	NO_TEST=1
23 22 26 7	IN	MEM_A_CLK_N<1..0>	NO_TEST=1
23 22 128	IN	MEM_A_DQ<63..0>	NO_TEST=1
23 22 128	IN	MEM_A_DQS_P<7..0>	NO_TEST=1
23 22 128	IN	MEM_A_DQS_N<7..0>	NO_TEST=1
23 22 26 7	IN	MEM_A_CKE<3..0>	NO_TEST=1
23 22 26 7	IN	MEM_A_CS_L<1..0>	NO_TEST=1
23 22 26 7	IN	MEM_A_ODT<1..0>	NO_TEST=1
23 22 26 7	IN	MEM_A_A<16..0>	NO_TEST=1
23 22 26 7	IN	MEM_A_BA<1..0>	NO_TEST=1
23 22 26 7	IN	MEM_A_BG<1..0>	NO_TEST=1
23 22 26	IN	MEM_A_PAR	NO_TEST=1
23 22 26	IN	MEM_A_ALERT_L	NO_TEST=1
23 22 26	IN	MEM_A_ACT_L	NO_TEST=1
25 24 26	IN	MEM_B_CLK_P<1..0>	NO_TEST=1
25 24 26 7	IN	MEM_B_CLK_N<1..0>	NO_TEST=1
25 24 128	IN	MEM_B_DQ<63..0>	NO_TEST=1
25 24 128	IN	MEM_B_DQS_P<7..0>	NO_TEST=1
25 24 128	IN	MEM_B_DQS_N<7..0>	NO_TEST=1
25 24 26 7	IN	MEM_B_CKE<3..0>	NO_TEST=1
25 24 26 7	IN	MEM_B_CS_L<1..0>	NO_TEST=1
25 24 26 7	IN	MEM_B_ODT<1..0>	NO_TEST=1
25 24 26 7	IN	MEM_B_A<16..0>	NO_TEST=1
25 24 26 7	IN	MEM_B_BA<1..0>	NO_TEST=1
25 24 26 7	IN	MEM_B_BG<1..0>	NO_TEST=1
25 24 26 7	IN	MEM_B_PAR	NO_TEST=1
25 24 26 7	IN	MEM_B_ALERT_L	NO_TEST=1
25 24 26 7	IN	MEM_B_ACT_L	NO_TEST=1

DP X

27	IN	DP_X_SNK0_ML_P<3..0>	NO_TEST=1
27	IN	DP_X_SNK0_ML_N<3..0>	NO_TEST=1
97 27	IN	DP_X_SNK0_ML_C_P<3..0>	NO_TEST=1
97 27	IN	DP_X_SNK0_ML_C_N<3..0>	NO_TEST=1
27	IN	DP_X_SNK1_ML_P<3..0>	NO_TEST=1
27	IN	DP_X_SNK1_ML_N<3..0>	NO_TEST=1
98 27	IN	DP_X_SNK1_ML_C_P<3..0>	NO_TEST=1
98 27	IN	DP_X_SNK1_ML_C_N<3..0>	NO_TEST=1
27	IN	DP_X_SNK0_AUXCH_P	
27	IN	DP_X_SNK0_AUXCH_N	
98 27	IN	DP_X_SNK0_AUXCH_C_P	
98 27	IN	DP_X_SNK0_AUXCH_C_N	
95 27	IN	DP_X_SNK0_HPD	
30 27	IN	DP_XA_HPD	
27	IN	DP_X_SNK1_AUXCH_P	
27	IN	DP_X_SNK1_AUXCH_N	
98 27	IN	DP_X_SNK1_AUXCH_C_P	
98 27	IN	DP_X_SNK1_AUXCH_C_N	
95 27	IN	DP_X_SNK1_HPD	
31 27	IN	DP_XB_HPD	

H9M ESPI

39 12	IN	ESPI_CLK60M_PCH	NO_TEST=1
39 12 123	IN	ESPI_RESET_L	
39 12	IN	ESPI_IO<3..0>	NO_TEST=1
39 12	IN	ESPI_CS_L	NO_TEST=1
12	IN	PCH_ESPI_ALERT0_L	NO_TEST=1

DMI

13 5	IN	DMI_S2N_P<3..0>	NO_TEST=1
13 5	IN	DMI_S2N_N<3..0>	NO_TEST=1
13 5	IN	DMI_N2S_P<3..0>	NO_TEST=1
13 5	IN	DMI_N2S_N<3..0>	NO_TEST=1

PCH/WLANBT

36 14	IN	PCH_PCIE_WLAN_D2R_P	
36 14	IN	PCH_PCIE_WLAN_D2R_N	
36	IN	PCH_PCIE_WLAN_D2R_C_P	
36	IN	PCH_PCIE_WLAN_D2R_C_N	
36	IN	PCH_PCIE_WLAN_R2D_P	
36	IN	PCH_PCIE_WLAN_R2D_N	
36 14	IN	PCH_PCIE_WLAN_R2D_C_P	
36 14	IN	PCH_PCIE_WLAN_R2D_C_N	

PCH/SOC

41 14	IN	PCIE_SOC_D2R_P<3..0>	NO_TEST=1
41 14	IN	PCIE_SOC_D2R_N<3..0>	NO_TEST=1
41	IN	PCIE_SOC_D2R_C_P<3..0>	NO_TEST=1
41	IN	PCIE_SOC_D2R_C_N<3..0>	NO_TEST=1
47 41	IN	PCIE_SOC_R2D_P<3..0>	NO_TEST=1
47 41	IN	PCIE_SOC_R2D_N<3..0>	NO_TEST=1
47 14	IN	PCIE_SOC_R2D_C_P<3..0>	NO_TEST=1
47 14	IN	PCIE_SOC_R2D_C_N<3..0>	NO_TEST=1

USB2 HS D+/D-

30 14	IN	USB_UPC_PCH_XA_P	
30 14	IN	USB_UPC_PCH_XA_N	NO_TEST=1
31 14	IN	USB_UPC_PCH_XB_P	NO_TEST=1
31 14	IN	USB_UPC_PCH_XB_N	NO_TEST=1
121 110 14	IN	USB_UPC_PCH_TA_P	
121 110 14	IN	USB_UPC_PCH_TA_N	
121 111 14	IN	USB_UPC_PCH_TB_P	
121 111 14	IN	USB_UPC_PCH_TB_N	
30	IN	USB_UPC_PCH_XA_F_P	NO_TEST=1
30	IN	USB_UPC_PCH_XA_F_N	NO_TEST=1
31	IN	USB_UPC_XB_F_P	NO_TEST=1
31	IN	USB_UPC_XB_F_N	NO_TEST=1
110	IN	USB_UPC_PCH_TA_F_P	NO_TEST=1
110	IN	USB_UPC_PCH_TA_F_N	NO_TEST=1
111	IN	USB_UPC_PCH_TB_F_P	NO_TEST=1
111	IN	USB_UPC_PCH_TB_F_N	NO_TEST=1

DP T

107	IN	DP_T_SNK0_ML_P<3..0>	NO_TEST=1
107	IN	DP_T_SNK0_ML_N<3..0>	NO_TEST=1
107 98	IN	DP_T_SNK0_ML_C_P<3..0>	NO_TEST=1
107 98	IN	DP_T_SNK0_ML_C_N<3..0>	NO_TEST=1
107	IN	DP_T_SNK1_ML_P<3..0>	NO_TEST=1
107	IN	DP_T_SNK1_ML_N<3..0>	NO_TEST=1
107 98	IN	DP_T_SNK1_ML_C_P<3..0>	NO_TEST=1
107 98	IN	DP_T_SNK1_ML_C_N<3..0>	NO_TEST=1
107	IN	DP_T_SNK0_AUXCH_P	
107	IN	DP_T_SNK0_AUXCH_N	
107 98	IN	DP_T_SNK0_AUXCH_C_P	
107 98	IN	DP_T_SNK0_AUXCH_C_N	
107 95	IN	DP_T_SNK0_HPD	
110 107	IN	DP_TA_HPD	
107	IN	DP_T_SNK1_AUXCH_P	
107	IN	DP_T_SNK1_AUXCH_N	
107 98	IN	DP_T_SNK1_AUXCH_C_P	
107 98	IN	DP_T_SNK1_AUXCH_C_N	
107 95	IN	DP_T_SNK1_HPD	
111 107	IN	DP_TB_HPD	

CPU/PCH CLK (TP FOR PROTO BUILDS)

12 6	IN	CPU_CLK24M_NSSC_CLK_N	
12 6	IN	CPU_CLK24M_NSSC_CLK_P	
12 6	IN	CPU_CLK100M_PCIBCLK_N	
12 6	IN	CPU_CLK100M_PCIBCLK_P	
12 6	IN	CPU_CLK100M_BCLK_N	
12 6	IN	CPU_CLK100M_BCLK_P	
41 12 123	IN	PCIE_CLK100M_SOC_P	
41 12 123	IN	PCIE_CLK100M_SOC_N	
41 12	IN	SOC_CLKREQ_L	
36 12	IN	PCH_PCIE_CLK100M_WLAN_P	
36 12	IN	PCH_PCIE_CLK100M_WLAN_N	
19 12	IN	PCH_WLAN_CLKREQ_L	
	IN	EG_PEG_CLK100M_P	
	IN	EG_PEG_CLK100M_N	
19 12 120	IN	PCH_GPU_CLKREQ_L	
	IN	PCIE_CLK100M_DEBUG_P	
	IN	PCIE_CLK100M_DEBUG_N	
19 12 120	IN	PCH_GPU_CLKREQ_L	
27 12 123	IN	PCIE_CLK100M_TBT_X_P	
27 12 123	IN	PCIE_CLK100M_TBT_X_N	
19 12 27	IN	TBT_X_CLKREQ_L	
	IN	PCIE_CLK100M_TBT_T_P	
	IN	PCIE_CLK100M_TBT_T_N	
19 12 107	IN	TBT_T_CLKREQ_L	
20 18	IN	NC_ITPXDP_CLK100MN	
20 18	IN	NC_ITPXDP_CLK100MP	

USB-C X

32 27	IN	USBC_XA_D2R_P<2..1>	NO_TEST=1
32 27	IN	USBC_XA_D2R_N<2..1>	NO_TEST=1
32	IN	USBC_XA_D2R_R_P<2..1>	NO_TEST=1
32	IN	USBC_XA_D2R_R_N<2..1>	NO_TEST=1
32	IN	USBC_XA_D2R_CR_P<2..1>	NO_TEST=1
32	IN	USBC_XA_D2R_CR_N<2..1>	NO_TEST=1
32	IN	USBC_XA_R2D_P<2..1>	NO_TEST=1
32	IN	USBC_XA_R2D_N<2..1>	NO_TEST=1
32	IN	USBC_XA_R2D_C_P<2..1>	NO_TEST=1
32	IN	USBC_XA_R2D_C_N<2..1>	NO_TEST=1
32 27	IN	USBC_XA_R2D_CR_P<2..1>	NO_TEST=1
32 27	IN	USBC_XA_R2D_CR_N<2..1>	NO_TEST=1
30 27	IN	USBC_XA_AUXLSX1	
30 27	IN	USBC_XA_AUXLSX2	
32 27	IN	USBC_XB_D2R_P<2..1>	NO_TEST=1
32 27	IN	USBC_XB_D2R_N<2..1>	NO_TEST=1
32	IN	USBC_XB_D2R_R_P<2..1>	NO_TEST=1
32	IN	USBC_XB_D2R_R_N<2..1>	NO_TEST=1
32	IN	USBC_XB_D2R_CR_P<2..1>	NO_TEST=1
32	IN	USBC_XB_D2R_CR_N<2..1>	NO_TEST=1
32	IN	USBC_XB_R2D_P<2..1>	NO_TEST=1
32	IN	USBC_XB_R2D_N<2..1>	NO_TEST=1
32	IN	USBC_XB_R2D_C_P<2..1>	NO_TEST=1
32	IN	USBC_XB_R2D_C_N<2..1>	NO_TEST=1
32 27	IN	USBC_XB_R2D_CR_P<2..1>	NO_TEST=1
32 27	IN	USBC_XB_R2D_CR_N<2..1>	NO_TEST=1
31 27	IN	USBC_XB_AUXLSX1	
31 27	IN	USBC_XB_AUXLSX2	

USB-C T

107 112	IN	USBC_TA_D2R_P<2..1>	NO_TEST=1
107 112	IN	USBC_TA_D2R_N<2..1>	NO_TEST=1
112	IN	USBC_TA_D2R_R_P<2..1>	NO_TEST=1
112	IN	USBC_TA_D2R_R_N<2..1>	NO_TEST=1
112	IN	USBC_TA_D2R_CR_P<2..1>	NO_TEST=1
112	IN	USBC_TA_D2R_CR_N<2..1>	NO_TEST=1
112	IN	USBC_TA_R2D_P<2..1>	NO_TEST=1
112	IN	USBC_TA_R2D_N<2..1>	NO_TEST=1
112	IN	USBC_TA_R2D_C_P<2..1>	NO_TEST=1
112	IN	USBC_TA_R2D_C_N<2..1>	NO_TEST=1
107 112	IN	USBC_TA_R2D_CR_P<2..1>	NO_TEST=1
107 112	IN	USBC_TA_R2D_CR_N<2..1>	NO_TEST=1
107 110	IN	USBC_TA_AUXLSX1	
107 110	IN	USBC_TA_AUXLSX2	
107 112	IN	USBC_TB_D2R_P<2..1>	NO_TEST=1
107 112	IN	USBC_TB_D2R_N<2..1>	NO_TEST=1
112	IN	USBC_TB_D2R_R_P<2..1>	NO_TEST=1
112	IN	USBC_TB_D2R_R_N<2..1>	NO_TEST=1
112	IN	USBC_TB_D2R_CR_P<2..1>	NO_TEST=1
112	IN	USBC_TB_D2R_CR_N<2..1>	NO_TEST=1
112	IN	USBC_TB_R2D_P<2..1>	NO_TEST=1
112	IN	USBC_TB_R2D_N<2..1>	NO_TEST=1
112	IN	USBC_TB_R2D_C_P<2..1>	NO_TEST=1
112	IN	USBC_TB_R2D_C_N<2..1>	NO_TEST=1
107 112	IN	USBC_TB_R2D_CR_P<2..1>	NO_TEST=1
107 112	IN	USBC_TB_R2D_CR_N<2..1>	NO_TEST=1
107 111	IN	USBC_TB_AUXLSX1	
107 111	IN	USBC_TB_AUXLSX2	

H9M SSD NAND

91 90 89 88	IN	PCIE_SSD0_R2D_P<3..0>	NO_TEST=1
91 90 89 88	IN	PCIE_SSD0_R2D_N<3..0>	NO_TEST=1
91 90 89 88 41	IN	PCIE_SSD0_D2R_P<3..0>	NO_TEST=1
91 90 89 88 41	IN	PCIE_SSD0_D2R_N<3..0>	NO_TEST=1
91 90 89 88 41	IN	PCIE_SSD0_R2D_C_P<3..0>	NO_TEST=1
91 90 89 88 41	IN	PCIE_SSD0_R2D_C_N<3..0>	NO_TEST=1
91 90 89 88	IN	PCIE_SSD0_D2R_C_P<3..0>	NO_TEST=1
91 90 89 88	IN	PCIE_SSD0_D2R_C_N<3..0>	NO_TEST=1
86 85 84 83	IN	PCIE_SSD1_R2D_P<3..0>	NO_TEST=1
86 85 84 83	IN	PCIE_SSD1_R2D_N<3..0>	NO_TEST=1
86 85 84 83 41	IN	PCIE_SSD1_D2R_P<3..0>	NO_TEST=1
86 85 84 83 41	IN	PCIE_SSD1_D2R_N<3..0>	NO_TEST=1
86 85 84 83 41	IN	PCIE_SSD1_R2D_C_P<3..0>	NO_TEST=1
86 85 84 83 41	IN	PCIE_SSD1_R2D_C_N<3..0>	NO_TEST=1
86 85 84 83	IN	PCIE_SSD1_D2R_C_P<3..0>	NO_TEST=1
86 85 84 83	IN	PCIE_SSD1_D2R_C_N<3..0>	NO_TEST=1

XTAL

29 27	IN	TBT_X_XTAL25M_IN	NO_TEST=1
29 27	IN	TBT_X_XTAL25M_OUT	NO_TEST=1
109 107	IN	TBT_T_XTAL25M_IN	NO_TEST=1
109 107	IN	TBT_T_XTAL25M_OUT	NO_TEST=1
38	IN	SOC_XTAL24M_IN	NO_TEST=1
38	IN	SOC_XTAL24M_OUT	NO_TEST=1
38	IN	SOC_XTAL24M_OUT_R	NO_TEST=1
77	IN	PMU_XTAL1	NO_TEST=1
77	IN	PMU_XTAL1_R	NO_TEST=1
77	IN	PMU_XTAL2	NO_TEST=1
77 12	IN	PMU_CLK32K_PCH	NO_TEST=1
12	IN	PCH_CLK32K_RTCX1	
12	IN	PCH_CLK24M_XTALIN	NO_TEST=1
12	IN	PCH_CLK24M_XTALOUT	NO_TEST=1
12	IN	PCH_CLK24M_XTALOUT_R	NO_TEST=1
98	IN	GPU_XTALIN	

EG INT DP

98 95	IN	DP_INT_EG_ML_N<3..0>	NO_TEST=1
98 95	IN	DP_INT_EG_ML_P<3..0>	NO_TEST=1
98 95	IN	DP_INT_EG_AUX_N	
98 95	IN	DP_INT_EG_AUX_P	

WIFI

37	IN	50_0_ANT	NO_TEST=1
37	IN	50_1_ANT	NO_TEST=1
37	IN	50_2_ANT	NO_TEST=1
37	IN	50_0_COM	NO_TEST=1
37	IN	50_1_COM	NO_TEST=1
37	IN	50_2_COM	NO_TEST=1
37	IN	50_A_0_DIPLEXER	NO_TEST=1
37 36	IN	50_A_0_MATCH	NO_TEST=1
37	IN	50_G_0_DIPLEXER	NO_TEST=1
37 36	IN	50_G_0_MATCH	NO_TEST=1
37	IN	50_A_1_DIPLEXER	NO_TEST=1
37 36	IN	50_A_1_MATCH	NO_TEST=1
37	IN	50_G_1_DIPLEXER	NO_TEST=1
37 36	IN	50_G_1_MATCH	NO_TEST=1
37	IN	50_A_2_DIPLEXER	NO_TEST=1
37 36	IN	50_A_2_MATCH	NO_TEST=1
37 36	IN	50_G_2_MATCH	NO_TEST=1

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PAGE TITLE
High speed No Testpoints

Apple Inc.

DRAWING NUMBER 051-04492
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DFU AND FCT TESTPOINTS placed on top side of MLB, oppsite from CPU.

DEBUG PORT

TPC451	PCH_UART_DEBUG_R2D	15	29
TPC452	PCH_UART_DEBUG_D2R	15	29
TPC4F1	SMC_DEBUGPRT_TX	29	39
TPC4F2	SMC_DEBUGPRT_RX	29	39
TPC4H8	SOC_DEBUGPRT_RX	40	
TPC4H9	SOC_DEBUGPRT_TX	40	
TPC402	TP_JTAG_SOC_TDO	39	
TPC403	TP_JTAG_SOC_TDI	39	
TPC488	SMC_FIXTURE_MODE_L	47	
TPC400	SWD_SOC_SWCLK	29	30
TPC401	SWD_SOC_SWDIO	29	30
TPC407	I2C_UPC_SCL	39	51
TPC4E9	I2C_UPC_SDA	39	51
TPC4Z5	I2C_PWR_SCL	39	51
TPC406	I2C_PWR_SDA	39	51
TPC453			

SSD VREF

TPC4Q0	TP_SSD0_S4E0_ANI0_VREF	PLACE_NEAR=U9100.G12:10.MM	88
TPC4Q1	TP_SSD0_S4E0_ANI1_VREF	PLACE_NEAR=U9100.I4:12.MM	88
TPC4Q2	TP_SSD0_S4E1_ANI0_VREF	PLACE_NEAR=U9200.G12:10.MM	89
TPC4Q3	TP_SSD0_S4E1_ANI1_VREF	PLACE_NEAR=U9200.I4:12.MM	89
TPC4Q4	TP_SSD0_S4E2_ANI0_VREF	PLACE_NEAR=U9300.G12:10.MM	90
TPC4Q5	TP_SSD0_S4E2_ANI1_VREF	PLACE_NEAR=U9300.I4:10.MM	90
TPC4Q6	TP_SSD0_S4E3_ANI0_VREF	PLACE_NEAR=U9400.G12:10.MM	91
TPC4Q7	TP_SSD0_S4E3_ANI1_VREF	PLACE_NEAR=U9400.I4:10.MM	91
TPC4Q8	TP_SSD1_S4E0_ANI0_VREF	PLACE_NEAR=U8600.G12:10.MM	83
TPC4Q9	TP_SSD1_S4E0_ANI1_VREF	PLACE_NEAR=U8600.I4:11.MM	83
TPC4P0	TP_SSD1_S4E1_ANI0_VREF	PLACE_NEAR=U8700.G12:10.MM	84
TPC4P1	TP_SSD1_S4E1_ANI1_VREF	PLACE_NEAR=U8700.I4:11.MM	84
TPC4P2	TP_SSD1_S4E2_ANI0_VREF	PLACE_NEAR=U8800.G12:12.MM	85
TPC4P3	TP_SSD1_S4E2_ANI1_VREF	PLACE_NEAR=U8800.I4:10.MM	85
TPC4P4	TP_SSD1_S4E3_ANI0_VREF	PLACE_NEAR=U8900.G12:10.MM	86
TPC4P5	TP_SSD1_S4E3_ANI1_VREF	PLACE_NEAR=U8900.I4:10.MM	86

SOC & NON-CUSTOMER-FACING USB PORT 1

PLACE IN ACCESSIBLE BOARD AREA / LAYOUT TO MATCH FIXTURE POGO BLOCK

TPC454	SOC_USB_VBUS	29	38
TPC458	SOC_FORCE_DFU	29	30 38 77 135
TPC455	USB_SOC_P	30	38
TPC456	USB_SOC_N	30	38
TPC457	PMU_ACTIVE_READY	30	38 77 135
TPC459	SOC_DFU_STATUS	29	30 38 135
TPC462	SOC_DOCK_CONNECT	30	31 39
TPC463	SOC_SWD_MUX_SEL_PCH	15	
TPC408	USB3_TEST_D2R_N (OUT)	14	
TPC409	USB3_TEST_D2R_P (OUT)	14	
TPC410	USB3_TEST_R2D_N (IN)	14	
TPC411	USB3_TEST_R2D_P (IN)	14	
TPC412	DZC414 5.5V-0.28PF 0201-THICKSTNCL		
TPC413			
TPC414	DZC415 5.5V-0.28PF 0201-THICKSTNCL		
TPC415			
	DZC400 5.5V-0.28PF 0201-THICKSTNCL		
	DZC401 5.5V-0.28PF 0201-THICKSTNCL		
	DZC402 5.5V-0.28PF 0201-THICKSTNCL		
	DZC403 5.5V-0.28PF 0201-THICKSTNCL		
TPC416	USB_UPC_PCH_TA_N (BI)	14	110 120
TPC417	USB_UPC_PCH_TA_P (BI)	14	110 120
	DZC408 5.5V-0.28PF 0201-THICKSTNCL		
	DZC409 5.5V-0.28PF 0201-THICKSTNCL		

NON-CUSTOMER-FACING USB PORT 2

PLACE IN ACCESSIBLE BOARD AREA / LAYOUT TO MATCH FIXTURE POGO BLOCK

TPC422	USB3_TEST2_D2R_N (OUT)	14	
TPC423	USB3_TEST2_D2R_P (OUT)	14	
TPC424	USB3_TEST2_R2D_N (IN)	14	
TPC425	USB3_TEST2_R2D_P (IN)	14	
TPC426	DZC410 5.5V-0.28PF 0201-THICKSTNCL		
TPC427			
TPC428	DZC411 5.5V-0.28PF 0201-THICKSTNCL		
TPC429			
	DZC412 5.5V-0.28PF 0201-THICKSTNCL		
	DZC413 5.5V-0.28PF 0201-THICKSTNCL		
TPC419	USB_UPC_PCH_TB_N (BI)	14	111 120
TPC420	USB_UPC_PCH_TB_P (BI)	14	111 120
	DZC406 5.5V-0.28PF 0201-THICKSTNCL		
	DZC407 5.5V-0.28PF 0201-THICKSTNCL		

DCI

PLACE IN ACCESSIBLE BOARD AREA / LAYOUT TO MATCH FIXTURE POGO BLOCK

TPC4N0	USB3_EXTA_D2R_P (BI)	14	29
TPC4N1	USB3_EXTA_D2R_N (BI)	14	29
TPC4N2	USB3_EXTA_R2D_P (BI)	29	
TPC4N3	USB3_EXTA_R2D_N (BI)	29	
TPC4N4			
TPC4N5	DZC416 5.5V-0.28PF 0201-THICKSTNCL		
TPC4N6			
TPC4N8			
	DZC417 5.5V-0.28PF 0201-THICKSTNCL		
	DZC418 5.5V-0.28PF 0201-THICKSTNCL		
	DZC419 5.5V-0.28PF 0201-THICKSTNCL		

BATTERY

TPC431	SYS_DETECT_L	67	
TPC432	I2C_PWR_SCL	51	67
TPC433	I2C_PWR_SDA	51	67
TPC434	TP_BMON_IOUT	67	
TPC435	PPVBAT_G3H_CONN	67	68 121
TPC436	PPVBAT_G3H_CONN	67	68 121
TPC437	PPVBAT_G3H_CONN	67	68 121
TPC4D5	PPVBAT_G3H_CONN	67	68 121
TPC4D6	PPVBAT_G3H_CONN	67	68 121
TPC4D7	PPVBAT_G3H_CONN	67	68 121
TPC4I7	PPVBAT_G3H_CONN	67	68 121
TPC4Z8	SYS_DETECT	67	
TPC4D8			
TPC4D9			
TPC4E0			
TPC4E1			
TPC4E2			
TPC440			
TPC4I6			

POWER SEQUENCING

TPC468	PPBUS_G3H	117 121 122
TPC441	PPBUS_HS_GPU	117 123 126
TPC492	PP3V3_G3H_SSD0_SNS	118
TPC491	PP3V3_G3H_T	65 118 123
TPC4C8	PMU_CLK32K_SOC	39 77 123
TPC404	PP1V8_SLPS2R	80 122 123
TPC4C1	PP1V8_AWAKE	66 80
TPC4C4	PP1V8_SLPS2R_PMUVDDGPIO	75
TPC4C0	PP1V1_SLPS2R	80
TPC4D1	PP0V8_SLPS2R	80
TPC4H1	PP0V82_SLPDDR	80 123
TPC4Z9	PP3V3_AWAKE	80
TPC4D2	PPVDDCPUSRAM_AWAKE	80
TPC4B8	PP0V9_SLPDDR	80
TPC4C5	P1V1_SLPDDR_SOCFET_EN	76 77 135
TPC4B9	PP1V1_SLPDDR	80
TPC4I5	PP1V2_AWAKE	80
TPC4B4	PPVDDCPU_AWAKE	80 123
TPC4C9	PMU_SYS_ALIVE	38 39 77 87 92 95
TPC4H0	PMU_COLD_RESET_L	39 64 77
TPC4H3	PMU_PVDDMAIN_EN	73 77
TPC4N7	P3V3MAIN_PGOOD	73 77
TPC4F8	PP3V0_G3H_RTC	80
TPC4G0	PCH_RTC_RESET_L	12 77
TPC4D0	P5VG3S_EN	73 77
TPC471	PP5V_G3S	118 122 123
TPC4H5	P3V3G3S_EN	77 79
TPC4H6	PP3V3_G3S_X	118
TPC495	PP3V3_G3H_SOCPMU	118
TPC4H7	P1V8G3S_EN	77 79 135
TPC489	PP1V8_G3S	47 49 118 122
TPC4D3	P5VG3S_PGOOD	73 77
TPC4C6	PMU_CLK32K_WLANBT_R	36 37 77
TPC4L1	SSD_PMU_RESET_L	38 47 87 92
TPC4I4	PP1V8_SSD0	88 89 90 91 92 126
TPC4I3	PP1V8_SSD1	83 84 85 86 87 126
TPC4I1	PP0V9_SSD0	88 89 90 91 92 126
TPC4I2	PP0V9_SSD1	83 84 85 86 87 126
TPC4L2	PP2V5_NAND_SSD0	88 89 90 91 92 123 126
TPC4I0	PP2V5_NAND_SSD1	83 84 85 86 87 123 126
TPC474	PMU_ONOFF_R_L	48
TPC444	PP3V3_S5	80
TPC4F7	PP1V8_S5	80
TPC486	PM_RSMRST_L	12 18 34 46 114
TPC4G2	PM_PWRBTN_L	18 80
TPC4B6	PVDDQ_EN_R	74
TPC442	PP2V5_S3	117 124 125
TPC469	PP1V2_S3	117 123 124 125
TPC481	PP1V05_S3	117
TPC4F4	PP1V05_S0SW	117
TPC4F5	PP1V2_S0SW	117
TPC4B7	PVCCIO_EN	77 78
TPC470	PPVCC_S0_CPU	117 123
TPC4L7	PPVCCGT_S0_CPU	117 123
TPC4F3	PPVCCSA_S0_CPU	117 123
TPC4L0	PPVCCIO_S0_CPU	117 123
TPC4F9	ALL_SYS_PWRGD	46 77
TPC4D4	CPUVR_PGOOD	77 80
TPC4F6	PP1V05_PRIM	117 123
TPC4L6	CPU_PWRGD	6 13
TPC4J1	SMC_SYSRST_L	39 46
TPC484	PM_PCH_PWROK	12 46
TPC482	PM_SYSRST_L	12 18 46
TPC483	PM_PCH_SYS_PWROK	12 46
TPC493	PP3V3_S0SW_TBT_X	118
TPC4J2	PP3V3_S0_GPU	117
TPC4J3	PP1V8_S0_GPU	58 93 94 97 98 99 103 105 115 116 123 126 127
TPC4J4	PP0V75_S0_GPU	99 105 115 123 124 126 127
TPC4J5	PPGFX_S0_GPU	58 99 100 104 123 126
TPC4J6	PPSOC_S0_GPU	58 99 104 123 126
TPC4J7	PP0V85_MEMCI_S0_GPU	99 105 115 126
TPC4J8	PP1V35_MEMIO_S0_GPU	93 94 99 101 105 115 123 126 127

BOM_COST_GROUP=DEBUG

STATUS AND RESETS

TPC4G8	ESPI_RESET_L	12	39 120
TPC4H4	UPC_PMU_RESET	29	67 77 109
TPC485	PLT_RST_L	12	20 35 46
TPC4G7	PM_MEMVTT_EN	5	74
TPC4G6	GPU_RESET_L	46	97 115 116
TPC4G5	DISP_GCON_RESET_L	119 95	
TPC405	SOC_SOCHOT_L	38	77
TPC4G1	PM_THRMTRIP_L	6	46
TPC4G3	CPU_PROCHOT_R_L	6	
TPC4G9	GFX_THROTTLE_L	98	
TPC477	PM_SLP_S5_L	12	
TPC476	PM_SLP_S4_L	12	
TPC475	PM_SLP_S3_L	12	14 27 107
TPC487	PM_SLP_S0_L	136 12	39 77 135
TPC4C7	SOC_WDOG	39	77
TPC4AH	GPU_GFX_OVERTEMP_R	46	
TPC4GA	GPU_VRAM_A_RST_L	93	101
TPC4GB	GPU_VRAM_B_RST_L	93	101
TPC4GC	GPU_VRAM_C_RST_L	94	102
TPC4GD	GPU_VRAM_D_RST_L	94	102

CHARGER

TPC4H2	CHGR_EN_MVR	67	68
TPC4Z6	PPVBAT_G3H_CHGR_REG	68	
TPC4Z7	PPDCIN_G3H_CHGR	68	124
TPC448			
TPC449			
TPC450			

CBAT TRIM

TPC4AC	PPBUS_G3H	117	121 122
TPC4AD			
TPC4AE			
TPC4AF			
TPC4AG			
TPC4AN			
TPC4AP			
TPC4AQ			
TPC4AR			
TPC4AS			

LEFT SIDE POWER INPUT (100W)

TPC4AA	PPDCIN_G3H	29	53 68 124
TPC4AB			
TPC4A5			
TPC4A6			
TPC4A7			
TPC4A8			
TPC4E5			
TPC4E6			
TPC4A0			
TPC4A1			
TPC4A9			
TPC4B0			
TPC4B1			
TPC4B2			
TPC4B3			
TPC4E7			
TPC4E8			
TPC4A2			
TPC4A3			
TPC496			

PAGE TITLE: DFU TEST POINTS

Apple Inc.

DRAWING NUMBER: 051-04492 SIZE: D

REVISION: 2.15.0

BRANCH

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FCT TEST POINTS (TOP SIDE OF MLB)

DFR/MESA

TPC503	DFR_DISP_VSYNC	50
TPC502	MIPI_DFR_CLK_CONN_FILT_P	50
TPC504	MIPI_DFR_CLK_CONN_FILT_N	50
TPC505	DFR_DISP_TE	40 50
TPC508	DFR_DISP_INT	38 50
TPC507	MIPI_DFR_DATA_CONN_FILT_P	50
TPC524	MIPI_DFR_DATA_CONN_FILT_N	50
TPC510	DFR_DISP_RESET_L	40 50
TPC534	I2C_DFR_SCL_R	52
TPC536	I2C_DFR_SDA_R	52
TPC522	DFR_LID_OPEN_L	50
TPC521	TP_DFR_TOUCH_PANEL_DETECT	50
TPC509	TP_DFR_TOUCH_RSVD	50
TPC529	SPI_DFR_CLK	47 50
TPC528	SPI_DFR_CS_L	40 50
TPC527	SPI_DFR_MISO_R	47 50
TPC530	SPI_DFR_MOSI	47 50
TPC533	DFR_TOUCH_INT_L	39 50
TPC535	DFR_TOUCH_CLK32K_RESET_L	40 50
TPC538	DFR_TOUCH_RESET_L	40 50
TPC539	TP_DFR_TOUCH_ROM_WC	50
TPC544	SPI_MESA_MISO_CONN	48
TPC546	MESA_INT_CONN	48
TPC548	MESA_BOOST_EN_CONN	48
TPC545	PMU_ONOFF_R_L_CONN	48
TPC550	SPI_MESA_CLK_CONN	48
TPC547	SPI_MESA_MOSI_CONN	48
TPC553	PMU_ONOFF_L	48 67 77 135
TPC540	PP1V8_SLPS2RSW_DFR	50 52
TPC541	PLACE_NEAR=J5110.17:10 MM PLACE_NEAR=J5100.21:10 MM	
TPC516	PP3V3_G3HSW_DFR	50
TPC518		
TPC500		
TPC501	PLACE_NEAR=J5110.26:10 MM	
TPC506	PLACE_NEAR=J5110.1:10 MM	
TPC511	PLACE_NEAR=J5100.6:10 MM PLACE_NEAR=J5100.23:15 MM	
TPC542	PP5V_G3S_DFR_FILT PLACE_NEAR=J5100.22:10 MM	50
TPC543	PP1V8_MESA_FILT_CONN PLACE_NEAR=J4900.1:10 MM	48
TPC552	PP16V0_MESA_FILT_CONN PLACE_NEAR=J4900.11:10 MM	48
TPC554	PP3V0_MESA_FILT_CONN PLACE_NEAR=J4900.13:10 MM	48
TPC555	PLACE_NEAR=J4900.15:15 MM	
NC_TP_J4900_8 (MAKE_BASE=TRUE)	NC_TP_J4900_8	48
NC_TP_J4900_10 (MAKE_BASE=TRUE)	NC_TP_J4900_10	48

TRACKPAD

TPC5Y1	I2C_TPAD_CONN_SCL	66
TPC5Y2	I2C_TPAD_CONN_SDA	66
TPC5Y0	TPAD_KBD_WAKE_L	47 66
TPC5Y3	SPI_TPAD_CLK_CONN	66
TPC5Y4	SPI_TPAD_CS_CONN_L	66
TPC5Y5	SPI_TPAD_MOSI_CONN	66
TPC5Y6	SPI_TPAD_MISO_CONN	66
TPC5Y7	SPI_TPAD_EN_CONN	66
TPC5Y8	SPI_TPAD_INT_CONN_L	66
TPC5Z8	IPD_LID_OPEN	47 50 64 66
TPC5X7	PPBUS_G3H PLACE_NEAR=J6800.33:10 MM	117 121
TPC5X8	PLACE_NEAR=J6800.40:10 MM	
TPC5X9	PP5V_G3S_TPAD_CONN PLACE_NEAR=J6800.15:10 MM	66
TPC5W0	PP3V3_G3S_T PLACE_NEAR=J6800.12:10 MM	118
TPC5W1	PP1V8_G3S_TPAD_CONN PLACE_NEAR=J6800.21:10 MM	66
TPC5W2	ACT_GND PLACE_NEAR=J6800.28:10 MM	66
TPC5W3	PLACE_NEAR=J6800.27:10 MM	
TPC5W4	PLACE_NEAR=J6800.16:10 MM	
TPC5W5	PLACE_NEAR=J6800.22:10 MM	
TPC5W6	PLACE_NEAR=J6800.23:10 MM	

FAN

TPC562	FAN_LT_PWM	59
TPC560	FAN_LT_TACH	59
TPC563	FAN_RT_PWM	59
TPC561	FAN_RT_TACH	59
TPC5Z3	PP5V_G3S PLACE_NEAR=J6001.1:10 MM	118 121 123
TPC5Z4	PLACE_NEAR=J6000.1:10 MM	
TPC5Z1	PLACE_NEAR=J6000.8:10 MM	
TPC5Z2	PLACE_NEAR=J6001.8:10 MM	

KEYBOARD

TPC567	PPVOUT_S0_KBDLED	81
TPC568	KBDLED_CATHODE1	81
TPC569	KBDLED_CATHODE2	81
TPC570	KBD_DRIVE_Y0	65
TPC571	KBD_DRIVE_Y1	65
TPC572	KBD_DRIVE_Y2	65
TPC573	KBD_DRIVE_Y3	65
TPC574	KBD_DRIVE_Y4	65
TPC575	KBD_DRIVE_Y5	65
TPC576	KBD_DRIVE_Y6	65
TPC577	KBD_DRIVE_Y7	65
TPC578	KBD_SENSE_X0	65
TPC579	KBD_SENSE_X1	65
TPC580	KBD_SENSE_X2	65
TPC581	KBD_SENSE_X3	65
TPC582	KBD_SENSE_X4	65
TPC583	KBD_SENSE_X5	65
TPC584	KBD_SENSE_X6	65
TPC585	KBD_SENSE_X7	65
TPC586	KBD_SENSE_X8	65
TPC587	KBD_SENSE_X9	65
TPC588	KBD_SENSE_X10	65
TPC589	KBD_SENSE_X11	65
TPC590	KBD_SENSE_X12	65
TPC5S0	KBD_ID1	65
TPC5S1	KBD_CAP_CATHODE	65
TPC5S2	KBD_RIGHT_SHIFT_KEY	65
TPC5S3	KBD_LEFT_OPTION_KEY	65
TPC5S4	KBD_CONTROL_KEY	65
TPC5S5	KBD_I2C_SCL	65 66
TPC5S6	KBD_I2C_SDA	65 66
TPC5S7	KBD_I2C_INT_L	65 66
TPC5S8	IOXP2_ADDR	65
TPC5S9	PMU_RSLOC_RST_L	65 67 77 135
TPC5V0	KBD_CAPSLOCK_LED	65
TPC5V1	CAPSLOCK_LED_EN	65
TPC5T2	PP3V3_G3H_RSLOC PLACE_NEAR=J6701.4:10 MM	65
TPC5T3	PP1V8_G3S PLACE_NEAR=J6701.30:10 MM	47 49 118 121
TPC5T4	PLACE_NEAR=J6701.31:10 MM	

DMIC AND AUDIO JACK

TPC592	AUD_DMIC0_CLK_CONN	47 64
TPC593	AUD_DMIC0_DATA_CONN	64
TPC595	AUD_DMIC1_CLK_CONN	47 64
TPC596	AUD_DMIC1_DATA_CONN	64
TPC594	PP1V8_DMIC PLACE_NEAR=J6640.3:10 MM	64
TPC597	PLACE_NEAR=J6640.6:10 MM	
TPC5A8	AUD_CONN_HP_LEFT	64
TPC5A9	AUD_CONN_HP_RIGHT	64
TPC5B0	AUD_CONN_RING2	64
TPC5B2	AUD_CONN_SLEEVE	64
TPC5B3	AUD_CONN_HP_SENSE_L	64
TPC5B5	AUD_CONN_HP_SENSE_R	64
TPC5B6	AUD_CONN_TIP_SENSE	64
TPC5B8	AUD_CONN_RING_SENSE	64
TPC5K1	AUD_CONN_SLEEVE_XW	64
TPC5B7	AUD_CONN_RING2_XW	64
TPC5A2	GND_AUDIO_CODEC	61 124
TPC5A7	PLACE_NEAR=J6600.23:10 MM	

EDP, CAMERA,ALS

TPC5C2	EDP_INT_AUX_P	82 95
TPC5C0	EDP_INT_AUX_N	82 95
TPC5C8	EDP_INT_ML_P<0>	82 95
TPC5C6	EDP_INT_ML_N<0>	82 95
TPC5D2	EDP_INT_ML_P<1>	82 95
TPC5D1	EDP_INT_ML_N<1>	82 95
TPC5D5	EDP_INT_ML_P<2>	82 95
TPC5D3	EDP_INT_ML_N<2>	82 95
TPC5E0	EDP_INT_ML_P<3>	82 95
TPC5D8	EDP_INT_ML_N<3>	82 95
TPC5F1	MIPI_FTCAM_CLK_CONN_P	82
TPC5E9	MIPI_FTCAM_CLK_CONN_N	82
TPC5E6	MIPI_FTCAM_DATA_CONN_P<0>	82
TPC5E4	MIPI_FTCAM_DATA_CONN_N<0>	82
TPC5C3	EDP_PANEL_PWR_BUF_EN	82
TPC5C5	DP_INT_HPD	82 95
TPC5C7	LCD_MUX_SEL	82 95
TPC5M1	BKLT_PWM_MLB2TCON	82
TPC5D9	I2C_BKLT_SCL	81 82
TPC5D7	I2C_BKLT_SDA	81 82
TPC5E3	I2C_TCON_SCL	51 82
TPC5E1	I2C_TCON_SDA	51 82
TPC5E8	I2C_ALS_SCL	40 52
TPC5E7	I2C_ALS_SDA	40 52
TPC5F0	I2C_CAM_ISOL_SCL	82
TPC5F2	I2C_CAM_ISOL_SDA	82
TPC5C1	PLACE_NEAR=J8500.11:10 MM	
TPC5C4	PLACE_NEAR=J8500.23:10 MM	
TPC5D0	PLACE_NEAR=J8500.32:10 MM	
TPC5D4	PLACE_NEAR=J8500.32:10 MM	
TPC5F3	PPVOUT_S0_LCDBKLT PLACE_NEAR=J8500.43:10 MM	81 82 124
TPC5F4	PP3V3_S0SW_LCD PLACE_NEAR=J8500.44:10 MM	51 82
TPC5F5	PLACE_NEAR=J8500.44:15 MM	
TPC5F6	PP5V_S0SW_LCD PLACE_NEAR=J8500.45:10 MM	82
TPC5F7	PP5V_S0_ALSCAM_F PLACE_NEAR=J8500.46:10 MM	82

MEMORY

TPC5I3	PVDDQ_PGOOD	74 77
TPC5I7	PP1V2_S3_CPUDDR	117 123
TPC5P8	PP0V6_S0_DDRVTT	117
TPC5P9	USFF_MEM_OK	15 135

DP SINK FORCING

TPC5L8	TBT_X_HDMI_DDC_CLK	29 98
TPC5L7	TBT_X_HDMI_DDC_DATA	29 98
TPC5N0	TBT_T_HDMI_DDC_CLK	98 109
TPC5L9	TBT_T_HDMI_DDC_DATA	98 109 113

DATA	CLK	ACTION (ON BOOT)
0	0	ONLY SNK0 AVAILABLE
0	1	NORMAL OPERATION
1	0	NO SNKS AVAILABLE
1	1	ONLY SNK1 AVAILABLE

SPEAKERS

TPC599	SPKRCONN_LT_OUTP	62
TPC5M4	PLACE_NEAR=J6400.5:10 MM	
TPC5M5	PLACE_NEAR=J6400.5:10 MM	
TPC598	SPKRCONN_LT_OUTN	62
TPC5G2	PLACE_NEAR=J6400.6:10 MM	
TPC5M3	PLACE_NEAR=J6400.6:10 MM	
TPC5Q0	SPKRCONN_LW1_OUTP	62
TPC5Q1	PLACE_NEAR=J6400.1:10 MM	
TPC5Q2	PLACE_NEAR=J6400.1:10 MM	
TPC5Q3	SPKRCONN_LW1_OUTN	62
TPC5Q4	PLACE_NEAR=J6400.2:10 MM	
TPC5Q5	PLACE_NEAR=J6400.2:10 MM	
TPC5Q6	SPKRCONN_LW2_OUTP	62
TPC5Q7	PLACE_NEAR=J6400.3:10 MM	
TPC5Q8	PLACE_NEAR=J6400.3:10 MM	
TPC5Q9	SPKRCONN_LW2_OUTN	62
TPC5R0	PLACE_NEAR=J6400.4:10 MM	
TPC5R1	PLACE_NEAR=J6400.4:10 MM	
TPC5R2	PLACE_NEAR=J6400.8:10 MM	
TPC5A4	SPKRCONN_RT_OUTP	63
TPC5L5	PLACE_NEAR=J6500.5:10 MM	
TPC5L6	PLACE_NEAR=J6500.5:10 MM	
TPC5A3	SPKRCONN_RT_OUTN	63
TPC5L3	PLACE_NEAR=J6500.6:10 MM	
TPC5L4	PLACE_NEAR=J6500.6:10 MM	
TPC5R3	SPKRCONN_RW1_OUTP	63
TPC5R4	PLACE_NEAR=J6500.1:10 MM	
TPC5R5	PLACE_NEAR=J6500.1:10 MM	
TPC5R6	SPKRCONN_RW1_OUTN	63
TPC5R7	PLACE_NEAR=J6500.2:10 MM	
TPC5R8	PLACE_NEAR=J6500.2:10 MM	
TPC5R9	SPKRCONN_RW2_OUTP	63
TPC5T5	PLACE_NEAR=J6500.3:12 MM	
TPC5T6	PLACE_NEAR=J6500.3:10 MM	
TPC5T7	SPKRCONN_RW2_OUTN	63
TPC5T8	PLACE_NEAR=J6500.4:10 MM	
TPC5T9	PLACE_NEAR=J6500.4:10 MM	
TPC5A6	PLACE_NEAR=J6500.8:10 MM	

USBC (PLACE NEAR CONNECTOR)

TPC5G4	USBC_XA_SBU1	30 32
TPC5G5	USBC_XA_SBU2	30 32
TPC5G6	USBC_XA_CC1	29 30 32
TPC5G7	USBC_XA_CC2	29 30 32
TPC5N3	TP_USBC_PP20V_XA	32
TPC5H0	PPVBUS_USBC_XA PLACE_NEAR=J3300.59:10 MM	29 30 124
TPC5I8	PLACE_NEAR=J3300.59:10 MM	
TPC5I9	PLACE_NEAR=J3300.60:10 MM	
TPC5J0	PLACE_NEAR=J3300.60:10 MM	
TPC5O5	USBC_XB_SBU1	31 32
TPC5O6	USBC_XB_SBU2	31 32
TPC5N9	USBC_XB_CC1	29 31 32
TPC5N8	USBC_XB_CC2	29 31 32
TPC5G3	TP_USBC_PP20V_XB	32
TPC5G9	PPVBUS_USBC_XB PLACE_NEAR=J3300.57:10 MM	29 31 123 124
TPC5J1	PLACE_NEAR=J3300.57:10 MM	
TPC5J2	PLACE_NEAR=J3300.58:10 MM	
TPC5J3	PLACE_NEAR=J3300.58:10 MM	
TPC5H5	PLACE_NEAR=J3300.83:10 MM	
TPC5H6	PLACE_NEAR=J3300.83:10 MM	
TPC5H7	PLACE_NEAR=J3300.86:10 MM	
TPC5H8	PLACE_NEAR=J3300.86:10 MM	
TPC5O7	USBC_TA_SBU1	110 112
TPC5O8	USBC_TA_SBU2	110 112
TPC5O1	USBC_TA_CC1	109 110 112
TPC5O2	USBC_TA_CC2	109 110 112
TPC5H2	TP_USBC_PP20V_TA	112
TPC5H4	PPVBUS_USBC_TA PLACE_NEAR=JB500.59:10 MM	109 110 124
TPC5J4	PLACE_NEAR=JB500.59:10 MM	
TPC5J5	PLACE_NEAR=JB500.60:10 MM	
TPC5J6	PLACE_NEAR=JB500.60:10 MM	
TPC5N1	USBC_TB_SBU1	111 112
TPC5N2	USBC_TB_SBU2	111 112
TPC5O3	USBC_TB_CC1	109 111 112
TPC5O4	USBC_TB_CC2	109 111 112
TPC5H1	TP_USBC_PP20V_TB	112
TPC5H3	PPVBUS_USBC_TB PLACE_NEAR=JB500.57:10 MM	109 111 124
TPC5J7	PLACE_NEAR=JB500.57:10 MM	
TPC5J8	PLACE_NEAR=JB500.58:10 MM	
TPC5J9	PLACE_NEAR=JB500.58:10 MM	
TPC5M2	PLACE_NEAR=JB500.83:10 MM	
TPC5K2	PLACE_NEAR=JB500.83:10 MM	
TPC5K3	PLACE_NEAR=JB500.86:10 MM	
TPC5K4	PLACE_NEAR=JB500.86:10 MM	
TPC5K5	USBC_XA_USB_TOP_P PLACE_NEAR=J3300.40:10 MM	30 32
TPC5K6	USBC_XA_USB_TOP_N PLACE_NEAR=J3300.42:10 MM	30 32
TPC5K7	USBC_XA_USB_BOT_P PLACE_NEAR=J3300.33:10 MM	30 32
TPC5K8	USBC_XA_USB_BOT_N PLACE_NEAR=J3300.31:10 MM	30 32

WIRELESS

TPC5H9	PP3V3_G3S_WLAN	118
TPC5I0	PP1V8_G3S_WLANBT	35 36 118

LID ANGLE SENSOR

TPC5I2	PP1V8_SLPS2R PLACE_NEAR=J4802.4:10 MM	
TPC5I1	SPI_AOP_MA781_CS_L	47
TPC5P0	SPI_AOP_MA781_CLK	47
TPC5P1	SPI_AOP_MA781_MISO	47
TPC5P2	SPI_AOP_MA781_MOSI	47
TPC5P3	ANGLE_SENSOR_MGL	47
TPC5P4	ANGLE_SENSOR_ND PLACE_NEAR=J4802.2:10 MM	47
TPC5Z5	PP3V3_G3H_RTC_X	118 123
TPC5L0	PLACE_NEAR=J4802.15:10 MM	

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JTAG

ACE

TPC600	TP-P5	TP_USBC_XA_RESET_L	29 30
TPC601	TP-P5	TP_USBC_TB_RESET_L	109
TPC602	TP-P5	UPC_XA_SER_DBG	30 33
TPC603	TP-P5	UPC_XB_SER_DBG	31 33
TPC604	TP-P5	UPC_TA_SER_DBG	110 113
TPC605	TP-P5	UPC_TB_SER_DBG	111 113
TPC606	TP-P5	UPC_XB_GPIO1	29 31
TPC627	TP-P5	UPC_TA_GPIO1	110
TPC629	TP-P5	UPC_TB_GPIO1	111
TPC607	TP-P5	TP_UPC_TA_GPIO9	110
TPC608	TP-P5	TP_UPC_TA_GPIO10	110
TPC609	TP-P5	TP_UPC_TB_GPIO9	111
TPC610	TP-P5	TP_UPC_TB_GPIO10	111

TBT

107 27 18 14	BI	JTAG_ISP_TCK	FUNC_TEST=TRUE
107 27 18 14	BI	JTAG_ISP_TDI	FUNC_TEST=TRUE
107 27 18	BI	JTAG_ISP_TDO	FUNC_TEST=TRUE
27 15	BI	JTAG_TBT_X_TMS	FUNC_TEST=TRUE
107 15	BI	JTAG_TBT_T_TMS	FUNC_TEST=TRUE
27	BI	TBT_X_TEST_EN	FUNC_TEST=TRUE
27	BI	TBT_X_TEST_PWR_GOOD	FUNC_TEST=TRUE
107	BI	TBT_T_TEST_EN	FUNC_TEST=TRUE
107	BI	TBT_T_TEST_PWR_GOOD	FUNC_TEST=TRUE

GPU

115 98	BI	GPU_JTAG_TESTEN	
115 98	BI	GPU_JTAG_TCK	
115 98	BI	GPU_JTAG_TDI	
115 98	BI	GPU_JTAG_TDO	
115 98	BI	GPU_JTAG_TMS	
115 98	BI	GPU_JTAG_TRST_L	
97	BI	GPU_RESET_R_L	
46	BI	GPU_RESET_L_R	

VRAM

94 93	BI	GPU_VRAM_TCK	
93	BI	GPU_VRAM_CONN_TDI	CKPLUS_WAIVE=SINGLE_NODENET
93	BI	GPU_VRAM_CONN_TDO	CKPLUS_WAIVE=SINGLE_NODENET
94 93	BI	GPU_VRAM_TMS	

SOC

38	BI	TP_JTAG_SOC_TRST_L	FUNC_TEST=TRUE
38	BI	SOC_JTAG_SEL	FUNC_TEST=TRUE
38	BI	SOC_TESTMODE	FUNC_TEST=TRUE

H9M BOUNDARY SCAN TESTPOINTS ON FCT TP PAGE

SSD BOUNDARY SCAN

91 90 89 88 39	IN	SSD0_SWCLK_UART_R2D	FUNC_TEST=TRUE
91 90 89 88 39	IN	SSD0_SWDIO_UART_D2R	FUNC_TEST=TRUE
86 85 84 83 39	IN	SSD1_SWCLK_UART_R2D	FUNC_TEST=TRUE
86 85 84 83 39	IN	SSD1_SWDIO_UART_D2R	FUNC_TEST=TRUE
91 90 89 88	IN	SSD0_S4E_JTAG_SEL	FUNC_TEST=TRUE
88	IN	SSD0_S4E0_JTAG_TDI	FUNC_TEST=TRUE
89 88	IN	SSD0_S4E0_JTAG_TDO	FUNC_TEST=TRUE
90 89	IN	SSD0_S4E1_JTAG_TDO	FUNC_TEST=TRUE
91 90	IN	SSD0_S4E2_JTAG_TDO	FUNC_TEST=TRUE
91	IN	SSD0_S4E3_JTAG_TDO	FUNC_TEST=TRUE
86 85 84 83	IN	SSD1_S4E_JTAG_SEL	FUNC_TEST=TRUE
83	IN	SSD1_S4E0_JTAG_TDI	FUNC_TEST=TRUE
86 84 83	IN	SSD1_S4E0_JTAG_TDO	FUNC_TEST=TRUE
86 85 84	IN	SSD1_S4E1_JTAG_TDO	FUNC_TEST=TRUE
86 85	IN	SSD1_S4E2_JTAG_TDO	FUNC_TEST=TRUE
86	IN	SSD1_S4E3_JTAG_TDO	FUNC_TEST=TRUE

TPC690 A	TP-P5	SSD0_S4E0_UART_TX	88
TPC691 A	TP-P5	SSD1_S4E0_UART_TX	83
TPC692 A	TP-P5	SSD0_S4E1_UART_TX	89
TPC693 A	TP-P5	SSD1_S4E1_UART_TX	84
TPC694 A	TP-P5	SSD0_S4E2_UART_TX	90
TPC695 A	TP-P5	SSD0_S4E3_UART_TX	91
TPC696 A	TP-P5	SSD1_S4E3_UART_TX	86
TPC697 A	TP-P5	SSD0_S4E1_DROOP_L	89
TPC698 A	TP-P5	SSD1_S4E2_UART_TX	85
TPC699 A	TP-P5	SSD0_CLKREQ2_L	41 47 90
TPC69A A	TP-P5	SSD0_S4E3_DROOP_L	91
TPC69B A	TP-P5	SSD0_S4E2_DROOP_L	90
TPC69C A	TP-P5	SSD0_CLKREQ3_L	41 47 91
TPC69D A	TP-P5	SSD0_S4E0_DROOP_L	88

KEYBOARD

TPC6H0	TP-P5	CAPSLOCK_LED_DRV	65
TPC6H1	TP-P5	KBD_RIGHT_SHIFT_L	65
TPC6H2	TP-P5	KBD_LEFT_OPTION_L	65
TPC6H3	TP-P5	KBD_CONTROL_L	65
TPC6H4	TP-P5	IOXP_I2C_SCL	65
TPC6H5	TP-P5	IOXP_I2C_SDA	65

EE TESTS SWE

TPC6F4	TP-P5	PVDD075GPU_ISNS_P	58 106
TPC6F5	TP-P5	PVDD075GPU_ISNS_N	58 106
TPC6F6	TP-P5	ISNS_GPU_1V8_P	58
TPC6F7	TP-P5	ISNS_GPU_1V8_N	58
TPC650	TP-P5	ISNS_HS_COMPUTING_P	53
TPC651	TP-P5	ISNS_HS_COMPUTING_N	53
TPC652	TP-P5	ISNS_HS_OTHER5V_P	53
TPC653	TP-P5	ISNS_HS_OTHER5V_N	53
TPC654	TP-P5	ISNS_HS_3V3_X_P	53
TPC655	TP-P5	ISNS_HS_3V3_X_N	53
TPC656	TP-P5	ISNS_HS_3V3_T_P	53
TPC657	TP-P5	ISNS_HS_3V3_T_N	53
TPC658	TP-P5	ISNS_LCDBKLT_P	53 81
TPC659	TP-P5	ISNS_LCDBKLT_N	53 81
TPC660	TP-P5	ISNS_1V0_P	54
TPC661	TP-P5	ISNS_1V0_N	54
TPC662	TP-P5	ISNS_CPUDDR_P	54 74
TPC663	TP-P5	ISNS_CPUDDR_N	54 74
TPC664	TP-P5	ISNS_CPUVDDQ_P	54
TPC665	TP-P5	ISNS_CPUVDDQ_N	54
TPC666	TP-P5	CPUVR_ISNS_P	54
TPC667	TP-P5	CPUVR_ISNS_N	54
TPC668	TP-P5	ISNS_WLAN_N	54
TPC669	TP-P5	ISNS_WLAN_P	54
TPC670	TP-P5	ISNS_WL1V8_P	54
TPC671	TP-P5	ISNS_WL1V8_N	54
TPC672	TP-P5	ISNS_LCDPANEL_P	55 82
TPC673	TP-P5	ISNS_LCDPANEL_N	55 82
TPC674	TP-P5	ISNS_CALPE_P	56
TPC675	TP-P5	ISNS_CALPE_N	56
TPC676	TP-P5	CPUGT_ISNS_R_P	56
TPC677	TP-P5	CPUGT_ISNS_R_N	56
TPC678	TP-P5	CPUSA_ISNS_P	56 71
TPC679	TP-P5	CPUSA_ISNS_N	56 71
TPC680	TP-P5	ISNS_CPUVCCIO_POS	56 78
TPC681	TP-P5	ISNS_CPUVCCIO_NEG	56 78
TPC683	TP-P5	PMU_GPU_GFX_ISENSE	59 96
TPC684	TP-P5	PMU_GPU_SOC_ISENSE	59 96
TPC685	TP-P5	EADC2_GPU_MEM_VDDCI_ISENSE	56 96
TPC686	TP-P5	EADC2_GPU_MEM_VDDIO_ISENSE	56 96
TPC687	TP-P5	GND_EADC1_COM	53 55 56 58
TPC688	TP-P5	SMC_DCIN_ISENSE	53 59
TPC689	TP-P5	SMC_BMON_ISENSE	53 59
TPC6G0	TP-P5	ISNS_TBT_X_P	56
TPC6G1	TP-P5	ISNS_TBT_X_N	56
TPC6G2	TP-P5	ISNS_2V5_S3_P	54 74
TPC6G3	TP-P5	ISNS_2V5_S3_N	54 74
TPC6G4	TP-P5	ISNS_TBT_T_P	56
TPC6G5	TP-P5	ISNS_TBT_T_N	56
TPC6G6	TP-P5	ISNS_KBDLED_P	55
TPC6G7	TP-P5	ISNS_KBDLED_N	55
TPC6G9	TP-P5	GND_SMC_AVSS	39 46 53 54 56 58
TPC6A2	TP-P5	ISNS_GPU_HS_P	58
TPC6A3	TP-P5	ISNS_GPU_HS_N	58
TPC6A4	TP-P5	SMC_PBUS_VSENSE	53 59
TPC6A5	TP-P5	PMU_CPU_VSENSE	58 59
TPC6A6	TP-P5	PMU_GPU_GFX_VSENSE	58 59
TPC6A7	TP-P5	EADC1_CPUGT_VSENSE	56 58
TPC6A8	TP-P5	GND_CALPE_AVSS	53 54 55 58 76 96
TPC6A9	TP-P5	EADC1_CPUSA_VSENSE	56 58
TPC6B0	TP-P5	PMU_GPU_SOC_VSENSE	58 59
TPC6B1	TP-P5	GND_EADC2_COM	54 55 56 58 96
TPC6B2	TP-P5	SMC_DCIN_VSENSE	53 59
TPC6B7	TP-P5	ISNS_PPBUS_MAIN_SSD0_P	55
TPC6B8	TP-P5	ISNS_PPBUS_MAIN_SSD0_N	55
TPC6B9	TP-P5	ISNS_PPBUS_MAIN_SSD1_P	55
TPC6C0	TP-P5	ISNS_PPBUS_MAIN_SSD1_N	55
TPC6C1	TP-P5	ISNS_P3V3_G3W_SSD0_P	55
TPC6C2	TP-P5	ISNS_P3V3_G3W_SSD0_N	55
TPC6C3	TP-P5	ISNS_P3V3_G3W_SSD1_P	55
TPC6C4	TP-P5	ISNS_P3V3_G3W_SSD1_N	55
TPC6C7	TP-P5	ISNS_T139_P	55
TPC6C8	TP-P5	ISNS_T139_N	55
TPC6L0	TP-P5	CHGR_CSO_R_P	68
TPC6L1	TP-P5	CHGR_CSO_R_N	68
TPC6L2	TP-P5	GFXGPU_SUM_R_P	96
TPC6L3	TP-P5	GFXGPU_SUM_R_N	96
TPC6L4	TP-P5	GPU_VDDCR_SOC_ISUM_P	103 104
TPC6L5	TP-P5	GPU_VDDCR_SOC_ISUM_N	103 104
TPC6L6	TP-P5	PVDDCIMEMGPU_ISUMP_RES	105
TPC6L7	TP-P5	PVDDCIMEMGPU_ISUMN_RES	105
TPC6L8	TP-P5	PVDDIOMEMGPU_ISNS1_P	105
TPC6L9	TP-P5	PVDDIOMEMGPU_ISNS1_N	105
TPC6B4	TP-P5	CHGR_CSI_R_P	68
TPC6B5	TP-P5	CHGR_CSI_R_N	68
TPC6B6	TP-P5	TP_SOC_TST_CLKOUT	38

PPC690 SM	P3MM	PMU_CLK32K_SOC	39 77 121
PPC657 SM	P3MM	PPVBUS_USBC_XB	29 31 122 124
PPC658 SM	P3MM	PPDCIN_XB_G3H_F	29 31
PPC659 SM	P3MM		
PPC660 SM	P3MM		

4 WIRE ICT

TPC6E0	TP-P5	VSNS_PPGFX_S0_GPU_POS	XW6E00 SM	PPGFX_S0_GPU	58 99 100 104 121 126
TPC6E1	TP-P5	VSNS_PPVCC_S0_CPU_POS	XW6E01 SM	PPVCC_S0_CPU	117 121
TPC6E2	TP-P5	VSNS_PPVCCGT_S0_CPU_POS	XW6E02 SM	PPVCCGT_S0_CPU	117 121
TPC6E3	TP-P5	VSNS_PPVCCSA_S0_CPU_POS	XW6E03 SM	PPVCCSA_S0_CPU	117 121
TPC6E4	TP-P5	VSNS_PPVDDCPU_AWAKE_POS	XW6E04 SM	PPVDDCPU_AWAKE	80 121
TPC6E5	TP-P5	VSNS_PP0V82_SLPDDR_POS	XW6E05 SM	PP0V82_SLPDDR	80 121
TPC6J0	TP-P5	VSNS_PP1V2_S3_CPUDDR_POS	XW6E12 SM	PP1V2_S3_CPUDDR	117 122
TPC6J1	TP-P5	VSNS_PP1V35_MEMIO_S0_GPU_POS	XW6E13 SM	PP1V35_MEMIO_S0_GPU	93 94 99 101 105 115 121 126 127
TPC6J2	TP-P5	VSNS_PPSOC_S0P_GPU_POS	XW6E14 SM	PPSOC_S0_GPU	58 99 104 121 126
TPC6J3	TP-P5	VSNS_PPVIN_S0_CPUVR_VIN_POS	XW6E15 SM	PPVIN_S0_CPUVR_VIN	69
TPCJ4	TP-P5	VSNS_PP3V3_G3H_T_POS	XW6E16 SM	PP3V3_G3H_T	65 118 121
TPC6J5	TP-P5	VSNS_PPVCCIO_S0_CPU_POS	XW6E17 SM	PPVCCIO_S0_CPU	117 121
TPC6J6	TP-P5	VSNS_PP0V75_S0_GPU_POS	XW6E18 SM	PP0V75_S0_GPU	99 106 115 121 124 126 127
TPC6K5	TP-P5	VSNS_PP1V05_PRIM_POS	XW6E27 SM	PP1V05_PRIM	117 121
TPC6K6	TP-P5	VSNS_PP1V2_S3_POS	XW6E28 SM	PP1V2_S3	117 121 124 125
TPC6K7	TP-P5	VSNS_PP1V8_S0_GPU_POS	XW6E29 SM	PP1V8_S0_GPU	121 126 127 87 88 94 97 98 99 103 105 115 116
TPC6K8	TP-P5	VSNS_PP1V8_S0_GPU_REG_POS	XW6E30 SM	PP1V8_S0_GPU_REG	58 106 126
TPC6K9	TP-P5	VSNS_PP1V8_SLPS2R_POS	XW6E31 SM	PP1V8_SLPS2R	80 121 122
TPC6M0	TP-P5	VSNS_PP2V5_NAND_SSD0_POS	XW6E32 SM	PP2V5_NAND_SSD0	88 89 90 91 92 121 126
TPC6M1	TP-P5	VSNS_PP2V5_NAND_SSD1_POS	XW6E33 SM	PP2V5_NAND_SSD1	83 84 85 86 87 121 126
TPC6M2	TP-P5	VSNS_PP3V3_G3H_RTC_X_POS	XW6E34 SM	PP3V3_G3H_RTC_X	118 122
TPC6M3	TP-P5	VSNS_PPVCCPRIMCORE_PRIM_REG_POS	XW6E35 SM	PPVCCPRIMCORE_PRIM_REG	118
TPC6M4	TP-P5	VSNS_PP5V_G3S_POS	XW6E36 SM	PP5V_G3S	118 121 122
TPC6M5	TP-P5	VSNS_PPBUS_HS_CPU_POS	XW6E37 SM	PPBUS_HS_CPU	117 124 126
TPC6M6	TP-P5	VSNS_PPBUS_HS_GPU_POS	XW6E38 SM	PPBUS_HS_GPU	117 121 126
TPC6M7	TP-P5	VSNS_PPBUS_HS_OTH5V_POS	XW6E39 SM	PPBUS_HS_OTH5V	117

TPC6E6	TP-P5	VSNS_PPGFX_S0_GPU_NEG	XW6E06 SM
TPC6E7	TP-P5	VSNS_PPVCC_S0_CPU_NEG	XW6E07 SM
TPC6E8	TP-P5	VSNS_PPVCCGT_S0_CPU_NEG	XW6E08 SM
TPC6E9	TP-P5	VSNS_PPVCCSA_S0_CPU_NEG	XW6E09 SM
TPC6F0	TP-P5	VSNS_PPVDDCPU_AWAKE_NEG	XW6E10 SM
TPC6F1	TP-P5	VSNS_PP0V82_SLPDDR_NEG	XW6E11 SM
TPC6J7	TP-P5	VSNS_PP1V2_S3_CPUDDR_NEG	XW6E19 SM
TPC6J8	TP-P5	VSNS_PP1V35_MEMIO_S0_GPU_NEG	XW6E20 SM
TPC6J9	TP-P5	VSNS_PPSOC_S0_GPU_NEG	XW6E21 SM
TPC6K0	TP-P5	VSNS_PPVIN_S0_CPUVR_VIN_NEG	XW6E22 SM
TPC6K1	TP-P5	VSNS_PP3V3_G3H_T_NEG	XW6E23 SM
TPC6K2	TP-P5	VSNS_PPVCCIO_S0_CPU_NEG	XW6E24 SM
TPC6K3	TP-P5	VSNS_PP0V75_S0_GPU_NEG	XW6E25 SM
TPC6K4	TP-P5	VSNS_PP1V05_PRIM_NEG	XW6E26 SM
TPC6M8	TP-P5	VSNS_PP1V2_S3_NEG	XW6E40 SM
TPC6M9	TP-P5	VSNS_PP1V8_S0_GPU_NEG	XW6E41 SM
TPC6N0	TP-P5	VSNS_PP1V8_S0_GPU_REG_NEG	XW6E42 SM
TPC6N1	TP-P5	VSNS_PP1V8_SLPS2R_NEG	XW6E43 SM
TPC6N2	TP-P5	VSNS_PP2V5_NAND_SSD0_NEG	XW6E44 SM
TPC6N3	TP-P5	VSNS_PP2V5_NAND_SSD1_NEG	XW6E45 SM
TPC6N4	TP-P5	VSNS_PP3V3_G3H_RTC_X_NEG	XW6E46 SM
TPC6N5	TP-P5	VSNS_PPVCCPRIMCORE_PRIM_REG_NEG	XW6E47 SM
TPC6N6	TP-P5	VSNS_PP5V_G3S_NEG	XW6E48 SM
TPC6N7	TP-P5	VSNS_PPBUS_HS_CPU_NEG	XW6E49 SM
TPC6N8	TP-P5	VSNS_PPBUS_HS_GPU_NEG	XW6E50 SM
TPC6N9	TP-P5	VSNS_PPBUS_HS_OTH5V_NEG	XW6E51 SM

CPU XDP & PCH

18 6	IN	XDP_CPU_TCK	FUNC_TEST=TRUE
18 13	IN	XDP_PCH_TCK	FUNC_TEST=TRUE
18 6	IN	XDP_CPU_TDI	FUNC_TEST=TRUE
18 6	IN	XDP_CPU_TDO	FUNC_TEST=TRUE
18 13 6	IN	XDP_CPU_TRST_L	FUNC_TEST=TRUE
18 6	IN	XDP_CPU_TMS	FUNC_TEST=TRUE
18 13	IN	XDP_PCH_TMS	FUNC_TEST=TRUE
18 13	IN	XDP_PCH_TDI	FUNC_TEST=TRUE
18 13	IN	XDP_PCH_TDO	FUNC_TEST=TRUE
18 13 6	IN	XDP_CPU_PREQ_L	FUNC_TEST=TRUE
18 13	IN	XDP_CPU_PRDY_L	FUNC_TEST=TRUE
46 39	BI	SMC_PCH_SYS_PWROK	FUNC_TEST=TRUE
46 39	BI	SMC_PCH_PWROK	FUNC_TEST=TRUE
18 13	IN	XDP_PCH_JTAGX	FUNC_TEST=TRUE
18 13	BI	PCH_ITP_PMODE	FUNC_TEST=TRUE

EE TESTS PCH

PPC620 SM	P3MM	PCIE_CLK100M_DEBUG_N	12 120
PPC621 SM	P3MM	PCIE_CLK100M_DEBUG_P	12 120
PPC633 SM	P3MM	PCIE_CLK100M_SOC_N PLACE_NEAR=U3900.G12:25MM	12 41 120
PPC634 SM	P3MM	PCIE_CLK100M_SOC_P PLACE_NEAR=U3900.G13:25MM	12 41 120
PPC635 SM	P3MM	EG_PEG_CLK100M_N PLACE_NEAR=UA000.AN12:25MM	12 119
PPC636 SM	P3MM	EG_PEG_CLK100M_P PLACE_NEAR=UA000.AN14:25MM	12 119
PPC637 SM	P3MM	PCIE_CLK100M_TBT_X_N PLACE_NEAR=UB000.T19:25MM	12 27 120
PPC638 SM	P3MM	PCIE_CLK100M_TBT_X_P PLACE_NEAR=UB000.V19:25MM	12 27 120
PPC639 SM	P3MM	PCIE_CLK100M_TBT_T_N PLACE_NEAR=UB000.T19:25MM	12 107 120
PPC640 SM	P3MM	PCIE_CLK100M_TBT_T_P PLACE_NEAR=UB000.V19:25MM	12 107 120

EE SWITCH NODES

PPC603	P3MM	PVDDCPUAWAKE_SW0	75
PPC604	P3MM	PVDDCPUAWAKE_SW1	75
PPC605	P3MM	PVDDCPUAWAKE_SW2	75
PPC606	P3MM	PVDDCPUAWAKE_SW3	75
PPC607	P3MM	PVCCPRIMCORE_SW0	75
PPC608	P3MM	PVCCPRIMCORE_SW1	75
PPC609	P3MM	P0V8SLPDDR_SW0	75
PPC610	P3MM	P0V8SLPDDR_SW1	75
PPC611	P3MM	P1V8SLPS2R_SW0	75
PPC612	P3MM	P1V1SLPS2R_SW0	75
PPC613	P3MM	P1V1SLPS2R_SW1	75
PPC614	P3MM	P0V9SLPDDR_SW0	75
PPC615	P3MM	P0V9SLPDDR_SW1	75
PPC616	P3MM	PVDDCPUSRAMAWAKE_SW0	75

WP ROMS

TPC6D1	TP-P5	TBT_X_ROM_WP_L	27
TPC6D2	TP-P5	TBT_T_ROM_WP_L	107
TPC6D3	TP-P5	GPU_ROM_WP_L	98
TPC6D4	TP-P5	SPI_SOCROM_WP_L	46

EE TESTS MIPI CAMERA

PPC666 SM	P3MM	MIPI_FTCAM_CLK_P PLACE_NEAR=U3900.B26:10mm	40 82
PPC667 SM	P3MM	MIPI_FTCAM_CLK_N PLACE_NEAR=U3900.A26:10mm	40 82
PPC668 SM	P3MM	MIPI_FTCAM_DATA_P<0> PLACE_NEAR=U3900.B27:10mm	40 82
PPC669 SM	P3MM	MIPI_FTCAM_DATA_N<0> PLACE_NEAR=U3900.A27:10mm	40 82

EE TESTS SSD0

PPC642	P3MM	PCIE_CLK100M_SSD0_01_P	41 88 89
PPC643	P3MM	PCIE_CLK100M_SSD0_01_N	41 88 89
PPC644	P3MM	PCIE_CLK100M_SSD0_23_P	41 90 91
PPC645	P3MM	PCIE_CLK100M_SSD0_23_N	41 90 91
PPC646	P3MM	SSD0_CLKREQ0_L	41 47 88
PPC647	P3MM	SSD0_CLKREQ1_L	41 47 89

EE TESTS SSD1

PPC651	P3MM	PCIE_CLK100M_SSD1_01_P	41 83 84
PPC652	P3MM	PCIE_CLK100M_SSD1_01_N	41 83 84
PPC653	P3MM	PCIE_CLK100M_SSD1_23_P	41 85 86
PPC654	P3MM	PCIE_CLK100M_SSD1_23_N	41 85 86
PPC656	P3MM	SSD1_CLKREQ1_L	41 47 84

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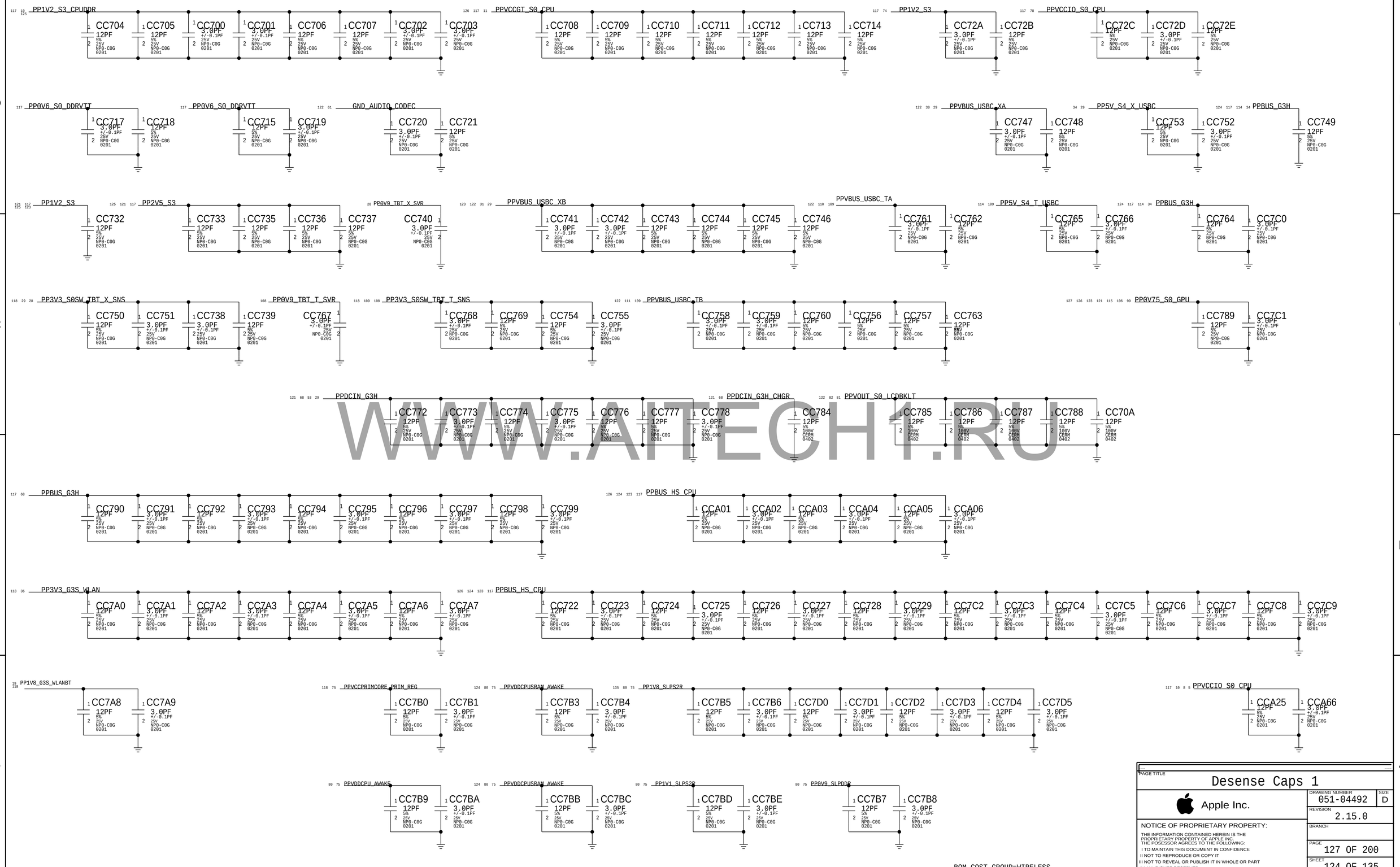

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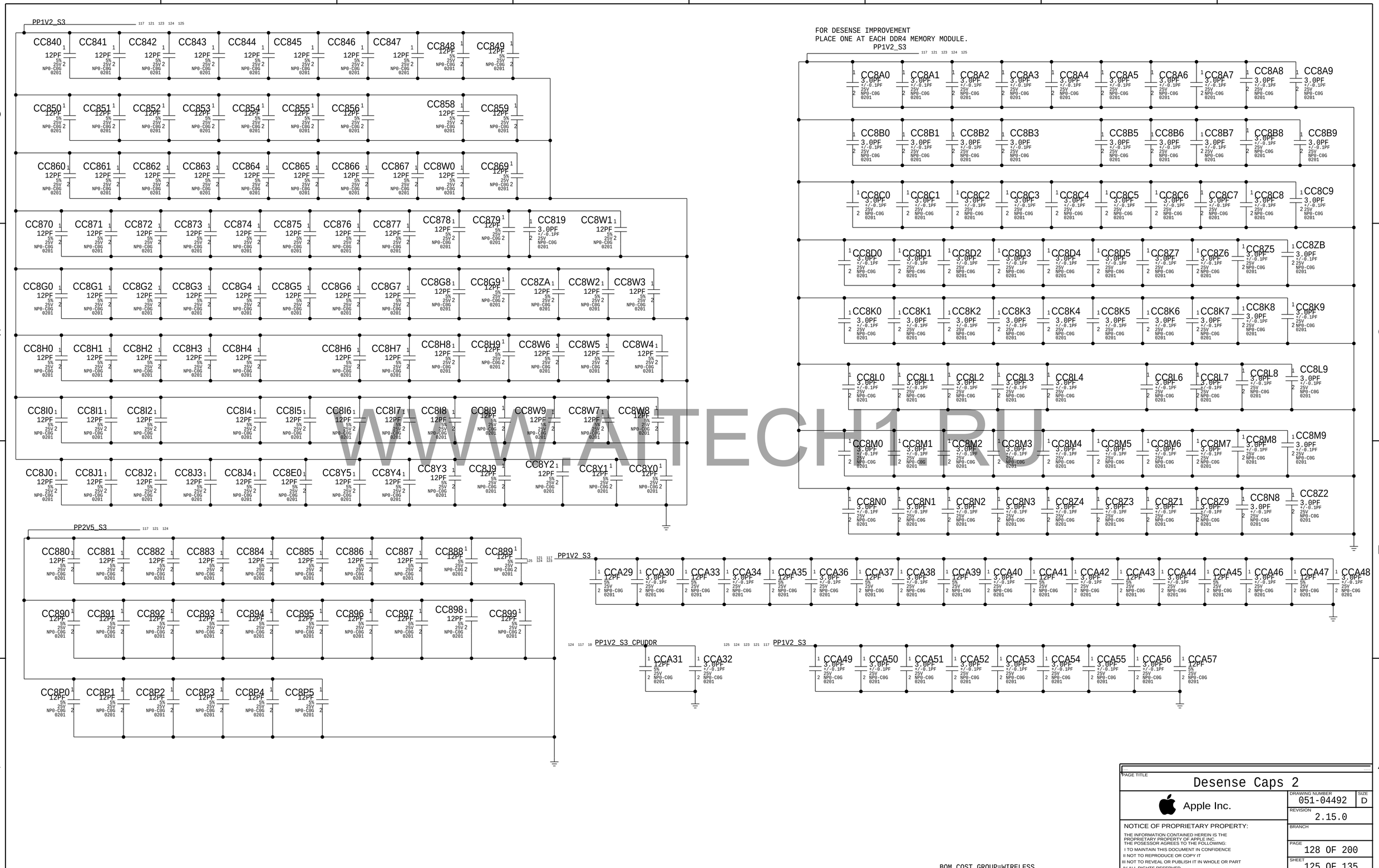

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Near NAND IC's

PP1V8_SSD0: CC900 12PF, CC901 3.0PF, CC902 12PF, CC903 3.0PF, CC904 12PF, CC905 3.0PF, CC906 12PF, CC907 3.0PF

Near NAND IC's

PP1V8_SSD1: CC918 12PF, CC919 3.0PF, CC91A 12PF, CC91B 3.0PF, CC91C 12PF, CC91D 3.0PF, CC91E 12PF, CC91F 3.0PF

Near NAND VR's

PP1V8_SSD0: CC930 12PF, CC931 3.0PF

PP1V8_SSD1: CC932 12PF, CC933 3.0PF

PP3V3_S0_GPU: CC9AB 12PF, CC9AC 3.0PF

PP0V9_SSD0: CC908 12PF, CC909 3.0PF, CC90A 12PF, CC90B 3.0PF, CC90C 12PF, CC90D 3.0PF, CC90E 12PF, CC90F 3.0PF

PP0V9_SSD1: CC920 12PF, CC921 3.0PF, CC922 12PF, CC923 3.0PF, CC924 12PF, CC925 3.0PF, CC926 12PF, CC927 3.0PF

PP0V9_SSD0: CC934 12PF, CC935 3.0PF

PP0V9_SSD1: CC936 12PF, CC937 3.0PF

PP1V8_S0_GPU_REG: CC9A3 12PF, CC9A4 3.0PF

PP2V5_NAND_SSD0: CC910 12PF, CC911 3.0PF, CC912 12PF, CC913 3.0PF, CC914 12PF, CC915 3.0PF, CC916 12PF, CC917 3.0PF, CC9F0 12PF, CC9F1 3.0PF

PP2V5_NAND_SSD1: CC928 12PF, CC929 3.0PF, CC92A 12PF, CC92B 3.0PF, CC92C 12PF, CC92D 3.0PF, CC92E 12PF, CC92F 3.0PF, CC9F2 12PF, CC9F3 3.0PF

PP2V5_NAND_SSD0: CC938 12PF, CC939 3.0PF

PP2V5_NAND_SSD1: CC93A 12PF, CC93B 3.0PF

PP0V75_S0_GPU: CC9AF 12PF, CC9B0 3.0PF

Near GMUX

PP3V3_S5: CC93C 12PF, CC93D 3.0PF, CC93E 12PF, CC93F 3.0PF

Near GPU

PPGFX_S0_GPU: CC940 12PF, CC941 3.0PF, CC942 12PF, CC943 3.0PF, CC944 12PF, CC945 3.0PF, CC946 12PF, CC947 3.0PF, CC948 12PF, CC949 3.0PF, CC94A 12PF, CC94B 3.0PF, CC94C 12PF, CC94D 3.0PF, CC94E 12PF, CC94F 3.0PF

Near GPU

PP0V75_S0_GPU: CC950 12PF, CC951 3.0PF, CC952 12PF, CC953 3.0PF

Near GPU

PPSOC_S0_GPU: CC954 12PF, CC955 3.0PF, CC956 12PF, CC957 3.0PF, CC958 12PF, CC959 3.0PF, CC95A 12PF, CC95B 3.0PF, CC95C 12PF, CC95D 3.0PF, CC95E 12PF, CC95F 3.0PF

Near GPU

PP0V85_MEMCI_S0_GPU: CC96A 12PF, CC96B 3.0PF, CC96C 12PF, CC96D 3.0PF, CC96E 12PF, CC96F 3.0PF

Near Power Shape Top Side

PPBUS_HS_CPU: CC970 12PF, CC971 3.0PF, CC972 12PF, CC973 3.0PF, CC974 12PF, CC975 3.0PF, CC976 12PF, CC977 3.0PF, CC978 12PF, CC979 3.0PF, CC97A 12PF, CC97B 3.0PF

Near GPU

PP1V35_MEMIO_S0_GPU: CC964 12PF, CC965 3.0PF, CC966 12PF, CC967 3.0PF, CC968 12PF, CC969 3.0PF

PPBUS_HS_GPU: CC97C 12PF, CC97D 3.0PF, CC97E 12PF, CC97F 3.0PF, CC980 12PF, CC981 3.0PF

PP1V8_S0_GPU: CC982 3.0PF, CC983 3.0PF, CC984 3.0PF, CC985 3.0PF, CC986 12PF, CC987 12PF, CC988 12PF, CC989 12PF

PP1V8_S0_GPU: CC98D 12PF, CC98E 3.0PF, CC98F 12PF, CC990 3.0PF

PPVCC_S0_CPU: CCA07 12PF, CCA08 3.0PF, CCA09 12PF, CCA10 3.0PF, CCA11 12PF, CCA12 3.0PF, CCA13 12PF, CCA14 3.0PF, CCA15 12PF, CCA16 3.0PF

PPBUS_HS_GPU: CC991 12PF, CC992 3.0PF, CC993 12PF, CC994 3.0PF, CC995 12PF, CC996 3.0PF, CC997 12PF, CC998 3.0PF, CC999 12PF, CC99A 3.0PF, CC99B 12PF, CC99C 3.0PF, CC99D 12PF, CC99E 3.0PF, CC99F 12PF, CC9A0 3.0PF, CC9A1 12PF, CC9A2 3.0PF, CC9BE 12PF, CC9BF 3.0PF, CC9C0 12PF, CC9C1 3.0PF, CC9C2 12PF, CC9C3 3.0PF, CC9C4 12PF, CC9C5 3.0PF

PP3V3_S5: CC9A5 12PF, CC9A6 3.0PF

PPVCCSA_S0_CPU: CC9AD 12PF, CC9AE 3.0PF, CCA23 12PF, CCA24 3.0PF

PPVCC_S0_CPU: CC9B1 3.0PF, CC9B2 3.0PF, CC9B3 3.0PF, CC9B4 3.0PF, CC9B5 3.0PF, CC9B6 3.0PF, CCA27 12PF, CCA28 3.0PF

PPGFX_S0_GPU: CC9A7 12PF, CC9A8 3.0PF

PPSOC_S0_GPU: CC9A9 12PF, CC9AA 3.0PF

PPVCCGT_S0_CPU: CCA17 12PF, CCA18 3.0PF, CCA19 12PF, CCA20 3.0PF, CCA21 12PF, CCA22 3.0PF, CC9B7 3.0PF, CC9B8 3.0PF, CC9B9 3.0PF, CC9BA 3.0PF, CC9BB 3.0PF, CC9BC 3.0PF, CC9BD 3.0PF

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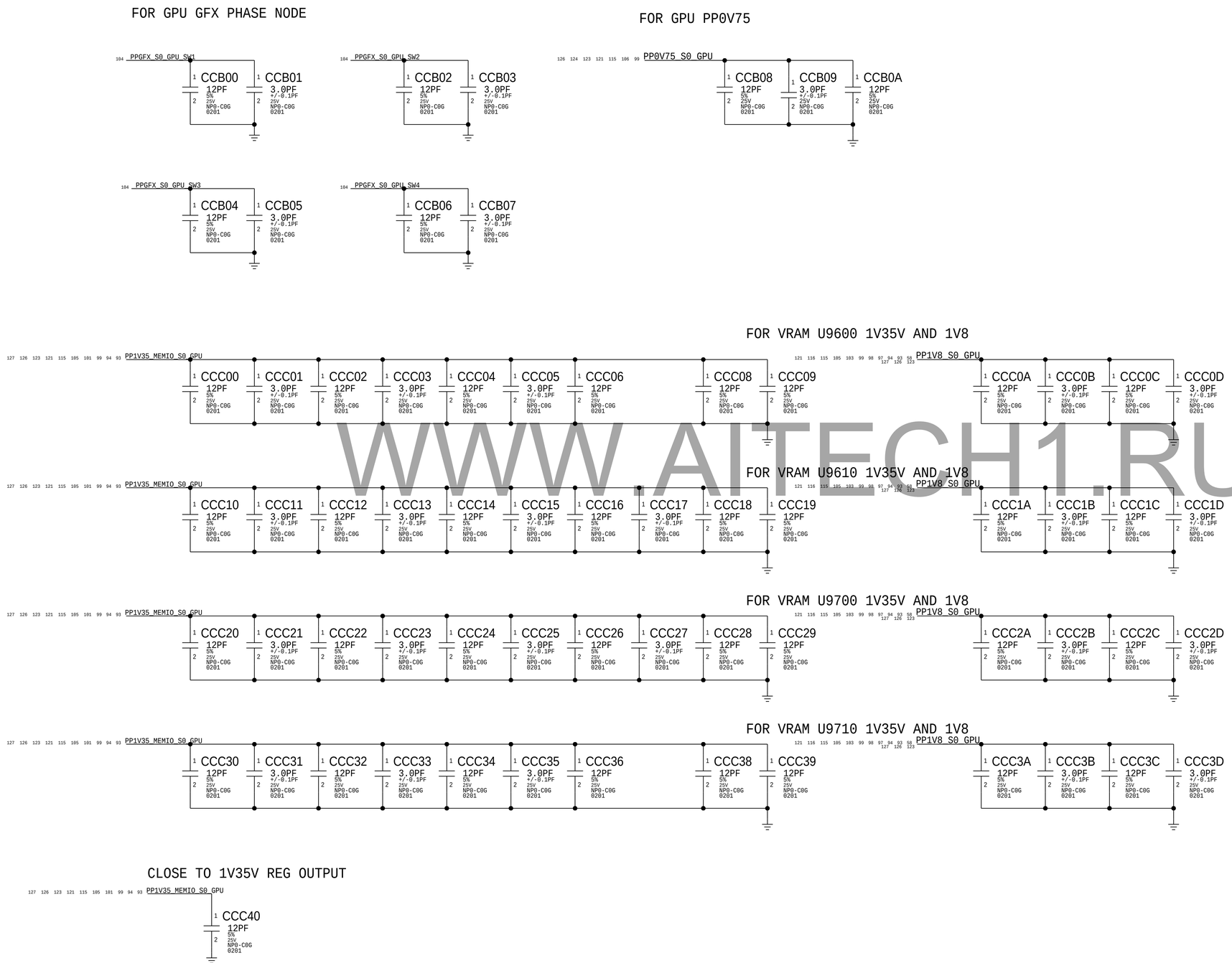

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DDR4 COMMAND/ADDRESS
Memory Bit/Byte Swizzle

MAKE_BASE=TRUE

		KBL-H DDR4 NET	BIT SWIZZLE	
120	22	MEM_A_DQ<0>	MEM_A_DQ<0>	7
120	22	MEM_A_DQ<1>	MEM_A_DQ<1>	7
120	22	MEM_A_DQ<2>	MEM_A_DQ<2>	7
120	22	MEM_A_DQ<3>	MEM_A_DQ<3>	7
120	22	MEM_A_DQ<4>	MEM_A_DQ<4>	7
120	22	MEM_A_DQ<5>	MEM_A_DQ<5>	7
120	22	MEM_A_DQ<6>	MEM_A_DQ<6>	7
120	22	MEM_A_DQ<7>	MEM_A_DQ<7>	7
120	22	MEM_A_DQ<8>	MEM_A_DQ<8>	7
120	22	MEM_A_DQ<9>	MEM_A_DQ<9>	7
120	22	MEM_A_DQ<10>	MEM_A_DQ<10>	7
120	22	MEM_A_DQ<11>	MEM_A_DQ<11>	7
120	22	MEM_A_DQ<12>	MEM_A_DQ<12>	7
120	22	MEM_A_DQ<13>	MEM_A_DQ<13>	7
120	22	MEM_A_DQ<14>	MEM_A_DQ<14>	7
120	22	MEM_A_DQ<15>	MEM_A_DQ<15>	7
120	22	MEM_A_DQ<16>	MEM_A_DQ<16>	7
120	22	MEM_A_DQ<17>	MEM_A_DQ<17>	7
120	22	MEM_A_DQ<18>	MEM_A_DQ<18>	7
120	22	MEM_A_DQ<19>	MEM_A_DQ<19>	7
120	22	MEM_A_DQ<20>	MEM_A_DQ<20>	7
120	22	MEM_A_DQ<21>	MEM_A_DQ<21>	7
120	22	MEM_A_DQ<22>	MEM_A_DQ<22>	7
120	22	MEM_A_DQ<23>	MEM_A_DQ<23>	7
120	22	MEM_A_DQ<24>	MEM_A_DQ<24>	7
120	22	MEM_A_DQ<25>	MEM_A_DQ<25>	7
120	22	MEM_A_DQ<26>	MEM_A_DQ<26>	7
120	22	MEM_A_DQ<27>	MEM_A_DQ<27>	7
120	22	MEM_A_DQ<28>	MEM_A_DQ<28>	7
120	22	MEM_A_DQ<29>	MEM_A_DQ<29>	7
120	22	MEM_A_DQ<30>	MEM_A_DQ<30>	7
120	22	MEM_A_DQ<31>	MEM_A_DQ<31>	7
120	23	MEM_A_DQ<32>	MEM_A_DQ<32>	7
120	23	MEM_A_DQ<33>	MEM_A_DQ<33>	7
120	23	MEM_A_DQ<34>	MEM_A_DQ<34>	7
120	23	MEM_A_DQ<35>	MEM_A_DQ<35>	7
120	23	MEM_A_DQ<36>	MEM_A_DQ<36>	7
120	23	MEM_A_DQ<37>	MEM_A_DQ<37>	7
120	23	MEM_A_DQ<38>	MEM_A_DQ<38>	7
120	23	MEM_A_DQ<39>	MEM_A_DQ<39>	7
120	23	MEM_A_DQ<40>	MEM_A_DQ<40>	7
120	23	MEM_A_DQ<41>	MEM_A_DQ<41>	7
120	23	MEM_A_DQ<42>	MEM_A_DQ<42>	7
120	23	MEM_A_DQ<43>	MEM_A_DQ<43>	7
120	23	MEM_A_DQ<44>	MEM_A_DQ<44>	7
120	23	MEM_A_DQ<45>	MEM_A_DQ<45>	7
120	23	MEM_A_DQ<46>	MEM_A_DQ<46>	7
120	23	MEM_A_DQ<47>	MEM_A_DQ<47>	7
120	23	MEM_A_DQ<48>	MEM_A_DQ<48>	7
120	23	MEM_A_DQ<49>	MEM_A_DQ<49>	7
120	23	MEM_A_DQ<50>	MEM_A_DQ<50>	7
120	23	MEM_A_DQ<51>	MEM_A_DQ<51>	7
120	23	MEM_A_DQ<52>	MEM_A_DQ<52>	7
120	23	MEM_A_DQ<53>	MEM_A_DQ<53>	7
120	23	MEM_A_DQ<54>	MEM_A_DQ<54>	7
120	23	MEM_A_DQ<55>	MEM_A_DQ<55>	7
120	23	MEM_A_DQ<56>	MEM_A_DQ<56>	7
120	23	MEM_A_DQ<57>	MEM_A_DQ<57>	7
120	23	MEM_A_DQ<58>	MEM_A_DQ<58>	7
120	23	MEM_A_DQ<59>	MEM_A_DQ<59>	7
120	23	MEM_A_DQ<60>	MEM_A_DQ<60>	7
120	23	MEM_A_DQ<61>	MEM_A_DQ<61>	7
120	23	MEM_A_DQ<62>	MEM_A_DQ<62>	7
120	23	MEM_A_DQ<63>	MEM_A_DQ<63>	7

MAKE_BASE=TRUE

		KBL-H DDR4 NET	BIT SWIZZLE	
120	24	MEM_B_DQ<0>	MEM_B_DQ<0>	7
120	24	MEM_B_DQ<1>	MEM_B_DQ<1>	7
120	24	MEM_B_DQ<2>	MEM_B_DQ<2>	7
120	24	MEM_B_DQ<3>	MEM_B_DQ<3>	7
120	24	MEM_B_DQ<4>	MEM_B_DQ<4>	7
120	24	MEM_B_DQ<5>	MEM_B_DQ<5>	7
120	24	MEM_B_DQ<6>	MEM_B_DQ<6>	7
120	24	MEM_B_DQ<7>	MEM_B_DQ<7>	7
120	24	MEM_B_DQ<8>	MEM_B_DQ<8>	7
120	24	MEM_B_DQ<9>	MEM_B_DQ<9>	7
120	24	MEM_B_DQ<10>	MEM_B_DQ<10>	7
120	24	MEM_B_DQ<11>	MEM_B_DQ<11>	7
120	24	MEM_B_DQ<12>	MEM_B_DQ<12>	7
120	24	MEM_B_DQ<13>	MEM_B_DQ<13>	7
120	24	MEM_B_DQ<14>	MEM_B_DQ<14>	7
120	24	MEM_B_DQ<15>	MEM_B_DQ<15>	7
120	24	MEM_B_DQ<16>	MEM_B_DQ<16>	7
120	24	MEM_B_DQ<17>	MEM_B_DQ<17>	7
120	24	MEM_B_DQ<18>	MEM_B_DQ<18>	7
120	24	MEM_B_DQ<19>	MEM_B_DQ<19>	7
120	24	MEM_B_DQ<20>	MEM_B_DQ<20>	7
120	24	MEM_B_DQ<21>	MEM_B_DQ<21>	7
120	24	MEM_B_DQ<22>	MEM_B_DQ<22>	7
120	24	MEM_B_DQ<23>	MEM_B_DQ<23>	7
120	24	MEM_B_DQ<24>	MEM_B_DQ<24>	7
120	24	MEM_B_DQ<25>	MEM_B_DQ<25>	7
120	24	MEM_B_DQ<26>	MEM_B_DQ<26>	7
120	24	MEM_B_DQ<27>	MEM_B_DQ<27>	7
120	24	MEM_B_DQ<28>	MEM_B_DQ<28>	7
120	24	MEM_B_DQ<29>	MEM_B_DQ<29>	7
120	24	MEM_B_DQ<30>	MEM_B_DQ<30>	7
120	24	MEM_B_DQ<31>	MEM_B_DQ<31>	7
120	25	MEM_B_DQ<32>	MEM_B_DQ<32>	7
120	25	MEM_B_DQ<33>	MEM_B_DQ<33>	7
120	25	MEM_B_DQ<34>	MEM_B_DQ<34>	7
120	25	MEM_B_DQ<35>	MEM_B_DQ<35>	7
120	25	MEM_B_DQ<36>	MEM_B_DQ<36>	7
120	25	MEM_B_DQ<37>	MEM_B_DQ<37>	7
120	25	MEM_B_DQ<38>	MEM_B_DQ<38>	7
120	25	MEM_B_DQ<39>	MEM_B_DQ<39>	7
120	25	MEM_B_DQ<40>	MEM_B_DQ<40>	7
120	25	MEM_B_DQ<41>	MEM_B_DQ<41>	7
120	25	MEM_B_DQ<42>	MEM_B_DQ<42>	7
120	25	MEM_B_DQ<43>	MEM_B_DQ<43>	7
120	25	MEM_B_DQ<44>	MEM_B_DQ<44>	7
120	25	MEM_B_DQ<45>	MEM_B_DQ<45>	7
120	25	MEM_B_DQ<46>	MEM_B_DQ<46>	7
120	25	MEM_B_DQ<47>	MEM_B_DQ<47>	7
120	25	MEM_B_DQ<48>	MEM_B_DQ<48>	7
120	25	MEM_B_DQ<49>	MEM_B_DQ<49>	7
120	25	MEM_B_DQ<50>	MEM_B_DQ<50>	7
120	25	MEM_B_DQ<51>	MEM_B_DQ<51>	7
120	25	MEM_B_DQ<52>	MEM_B_DQ<52>	7
120	25	MEM_B_DQ<53>	MEM_B_DQ<53>	7
120	25	MEM_B_DQ<54>	MEM_B_DQ<54>	7
120	25	MEM_B_DQ<55>	MEM_B_DQ<55>	7
120	25	MEM_B_DQ<56>	MEM_B_DQ<56>	7
120	25	MEM_B_DQ<57>	MEM_B_DQ<57>	7
120	25	MEM_B_DQ<58>	MEM_B_DQ<58>	7
120	25	MEM_B_DQ<59>	MEM_B_DQ<59>	7
120	25	MEM_B_DQ<60>	MEM_B_DQ<60>	7
120	25	MEM_B_DQ<61>	MEM_B_DQ<61>	7
120	25	MEM_B_DQ<62>	MEM_B_DQ<62>	7
120	25	MEM_B_DQ<63>	MEM_B_DQ<63>	7

MAKE_BASE

120	22	TRUE	MEM_A_DQS_P<0>	MEM_A_DQS_P<0>	7
120	22	TRUE	MEM_A_DQS_N<0>	MEM_A_DQS_N<0>	7
120	22	TRUE	MEM_A_DQS_P<1>	MEM_A_DQS_P<1>	7
120	22	TRUE	MEM_A_DQS_N<1>	MEM_A_DQS_N<1>	7
120	22	TRUE	MEM_A_DQS_P<2>	MEM_A_DQS_P<2>	7
120	22	TRUE	MEM_A_DQS_N<2>	MEM_A_DQS_N<2>	7
120	22	TRUE	MEM_A_DQS_P<3>	MEM_A_DQS_P<3>	7
120	22	TRUE	MEM_A_DQS_N<3>	MEM_A_DQS_N<3>	7
120	23	TRUE	MEM_A_DQS_P<4>	MEM_A_DQS_P<4>	7
120	23	TRUE	MEM_A_DQS_N<4>	MEM_A_DQS_N<4>	7
120	23	TRUE	MEM_A_DQS_P<5>	MEM_A_DQS_P<5>	7
120	23	TRUE	MEM_A_DQS_N<5>	MEM_A_DQS_N<5>	7
120	23	TRUE	MEM_A_DQS_P<6>	MEM_A_DQS_P<6>	7
120	23	TRUE	MEM_A_DQS_N<6>	MEM_A_DQS_N<6>	7
120	23	TRUE	MEM_A_DQS_P<7>	MEM_A_DQS_P<7>	7
120	23	TRUE	MEM_A_DQS_N<7>	MEM_A_DQS_N<7>	7

MAKE_BASE

120	24	TRUE	MEM_B_DQS_P<0>	MEM_B_DQS_P<0>	7
120	24	TRUE	MEM_B_DQS_N<0>	MEM_B_DQS_N<0>	7
120	24	TRUE	MEM_B_DQS_P<1>	MEM_B_DQS_P<1>	7
120	24	TRUE	MEM_B_DQS_N<1>	MEM_B_DQS_N<1>	7
120	24	TRUE	MEM_B_DQS_P<2>	MEM_B_DQS_P<2>	7
120	24	TRUE	MEM_B_DQS_N<2>	MEM_B_DQS_N<2>	7
120	24	TRUE	MEM_B_DQS_P<3>	MEM_B_DQS_P<3>	7
120	24	TRUE	MEM_B_DQS_N<3>	MEM_B_DQS_N<3>	7
120	25	TRUE	MEM_B_DQS_P<4>	MEM_B_DQS_P<4>	7
120	25	TRUE	MEM_B_DQS_N<4>	MEM_B_DQS_N<4>	7
120	25	TRUE	MEM_B_DQS_P<5>	MEM_B_DQS_P<5>	7
120	25	TRUE	MEM_B_DQS_N<5>	MEM_B_DQS_N<5>	7
120	25	TRUE	MEM_B_DQS_P<6>	MEM_B_DQS_P<6>	7
120	25	TRUE	MEM_B_DQS_N<6>	MEM_B_DQS_N<6>	7
120	25	TRUE	MEM_B_DQS_P<7>	MEM_B_DQS_P<7>	7
120	25	TRUE	MEM_B_DQS_N<7>	MEM_B_DQS_N<7>	7

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BOM NUMBER	BOM NAME	BOM OPTIONS
639-08595	MLB,8C-2.4G,MC-16,ULA,SS-8GB,TS-1TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.4G,MEM:MC-16GB,GPU:ULA,VRAM:SS-8GB,SSD:TS-1TB
639-08596	MLB,8C-2.3G,HY-16,ULA,SS-4GB,WD-2TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.3G,MEM:HY-16GB,GPU:ULA,VRAM:SS-4GB,SSD:WD-2TB
639-08597	MLB,6C-2.6G,MC-16,PRA,SS-4GB,TS-2TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:6C-2.6G,MEM:MC-16GB,GPU:PRA,VRAM:SS-4GB,SSD:TS-2TB
639-08598	MLB,8C-2.4G,HY-32,ULA,MC-4GB,WD-8TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.4G,MEM:HY-32GB,GPU:ULA,VRAM:MC-4GB,SSD:WD-8TB
639-08599	MLB,6C-2.6G,MC-32,PRA,MC-4GB,SS-512,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:6C-2.6G,MEM:MC-32GB,GPU:PRA,VRAM:MC-4GB,SSD:SS-512
639-08600	MLB,8C-2.4G,MC-64,ULA,SS-8GB,HY-4TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.4G,MEM:MC-64GB,GPU:ULA,VRAM:SS-8GB,SSD:HY-4TB
639-08601	MLB,8C-2.4G,HY-16,ULA,SS-4GB,TS-512,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.4G,MEM:HY-16GB,GPU:ULA,VRAM:SS-4GB,SSD:TS-512
639-08602	MLB,8C-2.3G,HY-32,PRA,SS-4GB,WD-4TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.3G,MEM:HY-32GB,GPU:PRA,VRAM:SS-4GB,SSD:WD-4TB
639-08603	MLB,8C-2.3G,MC-64,ULA,MC-4GB,WD-8TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.3G,MEM:MC-64GB,GPU:ULA,VRAM:MC-4GB,SSD:WD-8TB
639-08604	MLB,6C-2.6G,HY-16,PRA,MC-4GB,TS-256,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:6C-2.6G,MEM:HY-16GB,GPU:PRA,VRAM:MC-4GB,SSD:TS-256
639-08605	MLB,8C-2.4G,MC-32,ULA,SS-8GB,WD-4TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.4G,MEM:MC-32GB,GPU:ULA,VRAM:SS-8GB,SSD:WD-4TB
639-08606	MLB,6C-2.6G,MC-64,ULA,SS-4GB,TS-512,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:6C-2.6G,MEM:MC-64GB,GPU:ULA,VRAM:SS-4GB,SSD:TS-512
639-08607	MLB,8C-2.3G,MC-32,PRA,SS-4GB,WD-1TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.3G,MEM:MC-32GB,GPU:PRA,VRAM:SS-4GB,SSD:WD-1TB
639-08608	MLB,8C-2.4G,HY-16,ULA,MC-4GB,TS-1TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.4G,MEM:HY-16GB,GPU:ULA,VRAM:MC-4GB,SSD:TS-1TB
639-08609	MLB,8C-2.3G,MC-16,PRA,MC-4GB,WD-8TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.3G,MEM:MC-16GB,GPU:PRA,VRAM:MC-4GB,SSD:WD-8TB
639-08610	MLB,8C-2.4G,HY-32,ULA,SS-8GB,WD-2TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.4G,MEM:HY-32GB,GPU:ULA,VRAM:SS-8GB,SSD:WD-2TB
639-08639	MLB,8C-2.4G,MC-16,PRA,MC-4GB,WD-512,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.4G,MEM:MC-16GB,GPU:PRA,VRAM:MC-4GB,SSD:WD-512
639-08640	MLB,6C-2.6G,HY-16,PRA,MC-4GB,WD-256,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:6C-2.6G,MEM:HY-16GB,GPU:PRA,VRAM:MC-4GB,SSD:WD-256
639-08641	MLB,6C-2.6G,HY-32,ULA,HY-8GB,WD-1TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:6C-2.6G,MEM:HY-32GB,GPU:ULA,VRAM:HY-8GB,SSD:WD-1TB
639-08840	MLB,8C-2.3G,HY-16,ULA,MC-4GB,TS-256,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.3G,MEM:HY-16GB,GPU:ULA,VRAM:MC-4GB,SSD:TS-256
639-08841	MLB,6C-2.6G,MC-16,PRA,SS-4GB,TS-256,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:6C-2.6G,MEM:MC-16GB,GPU:PRA,VRAM:SS-4GB,SSD:TS-256
639-08863	MLB,8C-2.3G,MC-16,ULA,MC-4GB,TS-1TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.3G,MEM:MC-16GB,GPU:ULA,VRAM:MC-4GB,SSD:TS-1TB
639-08916	MLB,6C-2.6G,MC-32,ULA,SS-4GB,TS-512,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:6C-2.6G,MEM:MC-32GB,GPU:ULA,VRAM:SS-4GB,SSD:TS-512
639-08917	MLB,8C-2.4G,HY-32,ULA,SS-8GB,HY-4TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.4G,MEM:HY-32GB,GPU:ULA,VRAM:SS-8GB,SSD:HY-4TB
639-08918	MLB,8C-2.3G,HY-32,ULA,MC-4GB,WD-8TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.3G,MEM:HY-32GB,GPU:ULA,VRAM:MC-4GB,SSD:WD-8TB
639-09008	MLB,8C-2.3G,HY-16,ULA,MC-4GB,TS-1TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.3G,MEM:HY-16GB,GPU:ULA,VRAM:MC-4GB,SSD:TS-1TB
639-09014	MLB,6C-2.6G,MC-16,PRA,SS-4GB,WD-256,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:6C-2.6G,MEM:MC-16GB,GPU:PRA,VRAM:SS-4GB,SSD:WD-256
639-09015	MLB,8C-2.3G,HY-16,ULA,MC-4GB,WD-512,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.3G,MEM:HY-16GB,GPU:ULA,VRAM:MC-4GB,SSD:WD-512
639-09016	MLB,6C-2.6G,MC-16,PRA,SS-4GB,WD-256,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:6C-2.6G,MEM:MC-16GB,GPU:PRA,VRAM:SS-4GB,SSD:WD-256
639-09017	MLB,6C-2.6G,MC-16,PRA,SS-4GB,WD-256,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:6C-2.6G,MEM:MC-16GB,GPU:PRA,VRAM:SS-4GB,SSD:WD-256
639-09018	MLB,8C-2.4G,HY-32,PRA,SS-4GB,WD-256,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.4G,MEM:HY-32GB,GPU:PRA,VRAM:SS-4GB,SSD:WD-256
639-09019	MLB,8C-2.3G,MC-32,PRA,MC-4GB,WD-512,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.3G,MEM:MC-32GB,GPU:PRA,VRAM:MC-4GB,SSD:WD-512
639-09020	MLB,8C-2.4G,HY-32,PRA,SS-4GB,WD-512,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.4G,MEM:HY-32GB,GPU:PRA,VRAM:SS-4GB,SSD:WD-512
639-09021	MLB,8C-2.3G,MC-64,PRA,SS-8GB,WD-1TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.3G,MEM:MC-64GB,GPU:PRA,VRAM:SS-8GB,SSD:WD-1TB
639-09022	MLB,8C-2.3G,MC-32,PRA,SS-8GB,WD-1TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.3G,MEM:MC-32GB,GPU:PRA,VRAM:SS-8GB,SSD:WD-1TB
639-09023	MLB,8C-2.4G,MC-64,ULA,HY-8GB,WD-1TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.4G,MEM:MC-64GB,GPU:ULA,VRAM:HY-8GB,SSD:WD-1TB
639-09024	MLB,8C-2.4G,MC-64,ULA,SS-8GB,WD-2TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.4G,MEM:MC-64GB,GPU:ULA,VRAM:SS-8GB,SSD:WD-2TB
639-09025	MLB,8C-2.4G,MC-64,ULA,SS-8GB,WD-4TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.4G,MEM:MC-64GB,GPU:ULA,VRAM:SS-8GB,SSD:WD-4TB

BOM NUMBER	BOM NAME	BOM OPTIONS
939-08060	MLB,NO CPU,NO GPU,NO SSD,X970	ALTERNATE,BOM_BASE,BOM_DEV
939-08061	MLB,CPU INTERPOSER,NO GPU,NO SSD,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:INTERPOSER
939-08062	MLB,NO CPU,GPU ADPTR VDDCR,NO SSD,X970	ALTERNATE,BOM_BASE,BOM_DEV,GPU:ADPTR_VDDCR
939-08063	MLB,NO CPU,GPU ADPTR VMEM,NO SSD,X970	ALTERNATE,BOM_BASE,BOM_DEV,GPU:ADPTR_VMEM
939-08197	MLB,6C-2.6G,MC-32,UFU,SS-8GB,WD-4TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:6C-2.6G,MEM:MC-32GB,GPU:UFU,VRAM:SS-8GB,SSD:WD-4TB
939-08198	MLB,6C-2.6G,MC-32,USU,SS-8GB,WD-4TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:6C-2.6G,MEM:MC-32GB,GPU:USU,VRAM:SS-8GB,SSD:WD-4TB
939-08199	MLB,8C-2.3G,HY-16,UFU,MC-4GB,TS-1TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.3G,MEM:HY-16GB,GPU:UFU,VRAM:MC-4GB,SSD:TS-1TB
939-08200	MLB,8C-2.3G,HY-16,USU,MC-4GB,TS-1TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.3G,MEM:HY-16GB,GPU:USU,VRAM:MC-4GB,SSD:TS-1TB
939-08201	MLB,8C-2.3G,HY-16,UFU,SS-4GB,TS-512,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.3G,MEM:HY-16GB,GPU:UFU,VRAM:SS-4GB,SSD:TS-512
939-08202	MLB,8C-2.3G,HY-16,USU,SS-4GB,TS-512,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.3G,MEM:HY-16GB,GPU:USU,VRAM:SS-4GB,SSD:TS-512
939-08203	MLB,6C-2.6G,HY-32,UFS,HY-8GB,WD-8TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:6C-2.6G,MEM:HY-32GB,GPU:UFS,VRAM:HY-8GB,SSD:WD-8TB
939-08204	MLB,6C-2.6G,HY-32,USS,HY-8GB,WD-8TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:6C-2.6G,MEM:HY-32GB,GPU:USS,VRAM:HY-8GB,SSD:WD-8TB
939-08312	MLB,8C-2.3G,MC-16,UFU,SS-8GB,TS-1TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.3G,MEM:MC-16GB,GPU:UFU,VRAM:SS-8GB,SSD:TS-1TB
939-08313	MLB,8C-2.3G,MC-16,USU,SS-8GB,TS-1TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.3G,MEM:MC-16GB,GPU:USU,VRAM:SS-8GB,SSD:TS-1TB
939-08203	MLB,6C-2.6G,HY-32,UFS,HY-8GB,WD-8TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:6C-2.6G,MEM:HY-32GB,GPU:UFS,VRAM:HY-8GB,SSD:WD-8TB
939-08204	MLB,6C-2.6G,HY-32,USS,HY-8GB,WD-8TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:6C-2.6G,MEM:HY-32GB,GPU:USS,VRAM:HY-8GB,SSD:WD-8TB
939-08312	MLB,8C-2.3G,MC-16,UFU,SS-8GB,TS-1TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.3G,MEM:MC-16GB,GPU:UFU,VRAM:SS-8GB,SSD:TS-1TB
939-08313	MLB,8C-2.3G,MC-16,USU,SS-8GB,TS-1TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.3G,MEM:MC-16GB,GPU:USU,VRAM:SS-8GB,SSD:TS-1TB
939-08336	MLB,8C-2.4G,MC-32,UFS,SS-8GB,WD-4TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.4G,MEM:MC-32GB,GPU:UFS,VRAM:SS-8GB,SSD:WD-4TB
939-08337	MLB,8C-2.4G,MC-32,USS,SS-8GB,WD-4TB,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:8C-2.4G,MEM:MC-32GB,GPU:USS,VRAM:SS-8GB,SSD:WD-4TB
939-08338	MLB,6C-2.6G,MC-64,USS,SS-4GB,TS-512,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:6C-2.6G,MEM:MC-64GB,GPU:USS,VRAM:SS-4GB,SSD:TS-512
939-08339	MLB,6C-2.6G,MC-64,UFS,SS-4GB,TS-512,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:6C-2.6G,MEM:MC-64GB,GPU:UFS,VRAM:SS-4GB,SSD:TS-512
939-08522	MLB,6C-2.6G,MC-32,USS,SS-4GB,TS-512,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:6C-2.6G,MEM:MC-32GB,GPU:USS,VRAM:SS-4GB,SSD:TS-512
939-08523	MLB,6C-2.6G,MC-32,UFS,SS-4GB,TS-512,X970	ALTERNATE,BOM_BASE,BOM_DEV,CPU:6C-2.6G,MEM:MC-32GB,GPU:UFS,VRAM:SS-4GB,SSD:TS-512

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Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S00046	197S00036	ANY	ALL	Epson w/ TXC
197S00047	197S00036	ANY	ALL	Kyocera w/ TXC
197S00048	197S00036	ANY	ALL	Murata w/ TXC
376S1080	376S0820	ANY	ALL	
152S00726	152S00592	ANY	ALL	
376S1053	376S0604	ANY	ALL	Diodes alt to Fairchild
353S00636	353S4037	ANY	ALL	
155S00007	155S0667	ANY	ALL	
376S1106	376S0678	ANY	ALL	Fairchild alt to Vishay
371S00127	371S00182	ANY	ALL	
152S00769	152S00659	ANY	ALL	
372S00016	372S00015	ANY	ALL	
107S00041	107S00039	ANY	ALL	
740S00041	740S0159	ANY	ALL	
311S00138	311S0436	ANY	ALL	
152S00725	152S00590	ANY	ALL	
152S00841	152S00238	ANY	ALL	
376S00219	376S00079	ANY	ALL	TI for Fairchild
311S00121	311S0398	ANY	ALL	
311S0596	311S0593	ANY	ALL	
353S3526	353S3528	ANY	ALL	
353S3527	353S3528	ANY	ALL	
197S00131	197S00116	ANY	ALL	
197S00117	197S00116	ANY	ALL	
197S00115	197S00116	ANY	ALL	
152S00398	152S00204	ANY	ALL	
152S00786	152S00344	ANY	ALL	
311S00165	311S00164	ANY	ALL	
128S00050	128S0351	ANY	ALL	
138S00047	138S00073	ANY	ALL	
353S01041	353S01042	ANY	ALL	
155S0665	155S00232	ANY	ALL	
740S00051	740S00050	ANY	ALL	
152S00724	152S00311	ANY	ALL	
155S0694	155S0387	ANY	ALL	
103S0321	103S0276	ANY	ALL	
740S0144	740S0118	ANY	ALL	
740S00028	740S0118	ANY	ALL	
138S00077	138S00035	ANY	ALL	
138S00093	138S00035	ANY	ALL	
138S00056	138S1100	ANY	ALL	
107S00015	107S00011	ANY	ALL	
155S00018	155S0664	ANY	ALL	Murata w/ Taiyo
152S00359	152S00253	ANY	ALL	Chillisin alt to Cyntec
311S00118	311S0489	ANY	ALL	
155S00365	155S00191	ANY	ALL	
107S00297	107S00344	ANY	ALL	48180417: Ocarina Thermistor
138S0660	138S0684	ANY	ALL	
138S0846	138S0811	ANY	ALL	
155S0914	155S0897	ANY	ALL	
155S00190	155S0897	ANY	ALL	
138S00117	138S00071	ANY	ALL	
353S01346	353S01320	ANY	ALL	
376S00281	376S1147	ANY	ALL	
353S4376	353S3384	ANY	ALL	
128S00105	128S00098	ANY	ALL	49344753: 100uF T-Poly Cap
376S00304	376S1187	ANY	ALL	
132S00202	132S00175	ANY	ALL	
377S00079	377S00077	ANY	ALL	
311S0426	311S00007	ANY	ALL	
376S00309	376S00074	ANY	ALL	
377S00165	377S00031	ANY	ALL	
152S01100	152S01102	ANY	ALL	
377S00166	377S00106	ANY	ALL	
353S02030	353S01993	ANY	ALL	47710053: TPAD LDO

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S00878	353S00599	ANY	ALL	
371S00190	371S00085	ANY	ALL	
107S0248	107S0250	ANY	ALL	
107S00033	107S00034	ANY	ALL	
107S00103	107S00058	ANY	ALL	Cyntec w/ Yageo
311S00013	311S0508	ANY	ALL	Part wi
132S00064	132S0409	ANY	ALL	
128S0364	128S0264	ANY	ALL	Kemet w/ Panasonic
128S00058	128S00098	ANY	ALL	NEC w/ Rohm
107S00071	107S00053	ANY	ALL	
102S00054	102S00053	ANY	ALL	
376S00086	376S0761	ANY	ALL	
107S00044	107S00076	ANY	ALL	
311S00195	311S00196	ANY	ALL	
740S00019	740S00007	ANY	ALL	Bourns w/ Polytronics
353S00852	353S4262	ANY	ALL	TI w/ OnSemi
138S0775	138S0860	ANY	ALL	
138S0789	138S0941	ANY	ALL	Murata w/ SS
152S00363	152S00048	ANY	ALL	
152S00415	152S00140	ANY	ALL	
155S00204	155S0731	ANY	ALL	
311S00060	311S0273	ANY	ALL	
128S00009	128S00093	ANY	ALL	
128S00103	128S00093	ANY	ALL	47539941: 33uF CAP
128S00106	128S00093	ANY	ALL	49355299: 27uF CAP
128S00107	128S00093	ANY	ALL	49355299: 27uF CAP
138S0738	138S1101	ANY	ALL	Samsung alt to Murata
107S00234	107S00235	ANY	ALL	
311S00156	311S00129	ANY	ALL	
155S0660	155S0513	ANY	ALL	
197S00120	197S00118	ANY	ALL	
152S00368	152S00269	ANY	ALL	
311S0271	311S00008	ANY	ALL	NXP w/ Diodes
311S00104	311S00091	ANY	ALL	
371S00170	371S00125	ANY	ALL	
128S00039	128S00038	ANY	ALL	
128S0302	128S00038	ANY	ALL	
138S1103	138S0719	ANY	ALL	
311S00180	311S00181	ANY	ALL	
152S00770	152S0857	ANY	ALL	
740S00033	740S00002	ANY	ALL	
155S00166	155S0391	ANY	ALL	
107S0249	107S0251	ANY	ALL	
155S00401	155S00067	ANY	ALL	
152S00369	152S00268	ANY	ALL	Cyntec w/ NEC
371S00074	371S0602	ANY	ALL	
138S0689	138S0701	ANY	ALL	
128S00087	128S00011	ANY	ALL	
128S00031	128S00011	ANY	ALL	
128S00026	128S00011	ANY	ALL	
152S00182	152S00703	ANY	ALL	
152S00705	152S00412	ANY	ALL	
376S00303	376S00012	ANY	ALL	
152S00864	152S00851	ANY	ALL	
311S00179	311S00166	ANY	ALL	
353S01505	353S01389	ANY	ALL	
353S01506	353S01404	ANY	ALL	
311S00057	311S0612	ANY	ALL	
377S0155	377S0184	ANY	ALL	
152S00403	152S00322	ANY	ALL	
311S00193	311S00192	ANY	ALL	
138S00229	138S00107	ANY	ALL	
371S0689	371S0416	ANY	ALL	
138S00106	138S0754	ANY	ALL	
138S00257	138S0754	ANY	ALL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
103S00248	103S00247	ANY	ALL	8.06k 0.1% Resistor
103S00250	103S00249	ANY	ALL	18.2k 0.1% Resistor
116S00006	116S0175	ANY	ALL	0Ohm Resistor
128S00094	128S00067	ANY	ALL	150uF POLY CAP
128S00069	128S00067	ANY	ALL	150uF POLY CAP
128S00065	128S00067	ANY	ALL	150uF POLY CAP
138S00097	138S0750	ANY	ALL	4.7uF CAP
131S00134	131S00041	ANY	ALL	31561601: 12pF Desense
107S00101	107S00005	ANY	ALL	31560708: 5mOhm
107S00087	107S00029	ANY	ALL	31560843: 5mOhm
107S00086	107S00056	ANY	ALL	31560937: 3mOhm
107S00100	107S00057	ANY	ALL	31561063: 2mOhm
107S0240	107S0255	ANY	ALL	31561401: 1mOhm
107S00139	107S0178	ANY	ALL	31561213: 220k Resistor
128S0296	128S0487	ANY	ALL	31561532: 47uF-PT
128S00012	128S0487	ANY	ALL	31561532: 47uF-PT
353S00750	353S00877	ANY	ALL	
353S00832	353S00525	ANY	ALL	IMVP SA
353S00831	353S00519	ANY	ALL	IMVP VCORE
152S00782	152S00772	ANY	ALL	IMVP CORE INDUCTOR
138S00105	138S00037	ANY	ALL	31563978: 10uF CER
138S0714	138S0713	ANY	ALL	31564912: 10uF
138S0648	138S0703	ANY	ALL	31564224: 4.7uF CER
138S00284	128S00136	ANY	ALL	47567111: 2.2uF CER
138S0715	138S0732	ANY	ALL	31565015: 1uF CER
152S00845	152S00815	ANY	ALL	
138S00111	138S00036	ANY	ALL	31563894: 20uF CER
138S00286	138S00036	ANY	ALL	47541665: 20uF CER
132S00012	132S0401	ANY	ALL	31563715: 0.22uF
138S00084	138S00060	ANY	ALL	31564055: 47uF CER
138S0739	138S0706	ANY	ALL	NEC w/ Vishay
138S0945	138S0706	ANY	ALL	NEC w/ Rohm
138S0641	138S0700	ANY	ALL	Murata w/ SS&Taiyo
138S0759	138S0762	ANY	ALL	
138S00049	138S0831	ANY	ALL	
107S00090	107S00055	ANY	ALL	
138S0863	138S0853	ANY	ALL	
376S00282	376S1128	ANY	ALL	
377S0077	377S0183	ANY	ALL	
371S00180	371S00077	ANY	ALL	NXP alt to Diodes
138S00104	138S0978	ANY	ALL	
138S00024	138S0986	ANY	ALL	
152S00434	152S1829	ANY	ALL	
197S00053	197S00050	ANY	ALL	Kyocera w/ TXC
197S00054	197S00050	ANY	ALL	NDK w/ TXC
197S00055	197S00050	ANY	ALL	Murata w/ TXC
335S00270	335S00203	ANY	ALL	Adesto for Micronix
155S00034	155S0706	ANY	ALL	Taiyo w/ Murata
353S00879	353S00754	ANY	ALL	
155S00203	155S0894	ANY	ALL	
152S00461	152S00112	ANY	ALL	
376S00146	376S1061	ANY	ALL	
152S01218	152S00413	ANY	ALL	50058507: 2.7uH IND
152S00199	152S00413	ANY	ALL	
335S00066	335S0946	ANY	ALL	
152S00707	152S00689	ANY	ALL	
311S00177	311S00178	ANY	ALL	
311S0562	311S0372	ANY	ALL	BUF
132S00176	132S0640	ANY	ALL	CAP
353S01792	353S3901	ANY	ALL	AMP
311S00112	311S0437	ANY	ALL	BUF
335S00410	335S00254	ANY	ALL	FUSE
152S01023	152S00384	ANY	ALL	IND
372S00033	372S00029	ANY	ALL	Themperature sensor
152S00705	152S00371	ANY	ALL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00371	152S00412	ANY	ALL	
197S00181	197S00106	ANY	ALL	
131S00299	131S00118	ANY	ALL	
131S00308	131S00037	ANY	ALL	
197S00143	197S00142	ANY	ALL	
132S00229	132S00010	ANY	ALL	
132S00230	132S00035	ANY	ALL	
138S0772	138S00013	ANY	ALL	
138S00086	138S0884	ANY	ALL	
311S00025	311S0539	ANY	ALL	
152S00708	152S00265	ANY	ALL	
138S00139	138S00138	ANY	ALL	47826168: GPU GFX VR DeCap
138S00164	138S00138	ANY	ALL	47826168: GPU GFX VR DeCap
197S00213	197S00190	ANY	ALL	47889287: GPU OSC
197S00229	197S00190	ANY	ALL	47889287: GPU OSC
152S01139	152S01107	ANY	ALL	47566674: GPU 1.8V Filter
116S00007	116S00006	ANY	ALL	48352711: Res 0R 3A
376S00036	376S00328	ANY	ALL	48352555: GPU MEM VR HS FET
376S00321	376S00397	ANY	ALL	48352623: GPU MEM VR LS FET
371S00064	371S00193	ANY	ALL	43721339: Schottky Diode
152S01176	152S01173	ANY	ALL	48689463: GPU MEMIO VR Ind
376S00373	376S1038	ANY	ALL	

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Alternate Parts Keyboard

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0786	138S0847	ANY	ALL	
131S00059	131S0852	ANY	ALL	
138S00087	138S1086	ANY	ALL	
152S00812	152S1701	ANY	ALL	
371S00217	371S00079	ANY	ALL	
353S00497	353S00796	ANY	ALL	
152S01024	152S00386	ANY	ALL	
152S00997	152S00476	ANY	ALL	
371S00220	371S00181	ANY	ALL	DIODE
353S01831	353S00519	ANY	ALL	
138S00181	138S0835	ANY	ALL	

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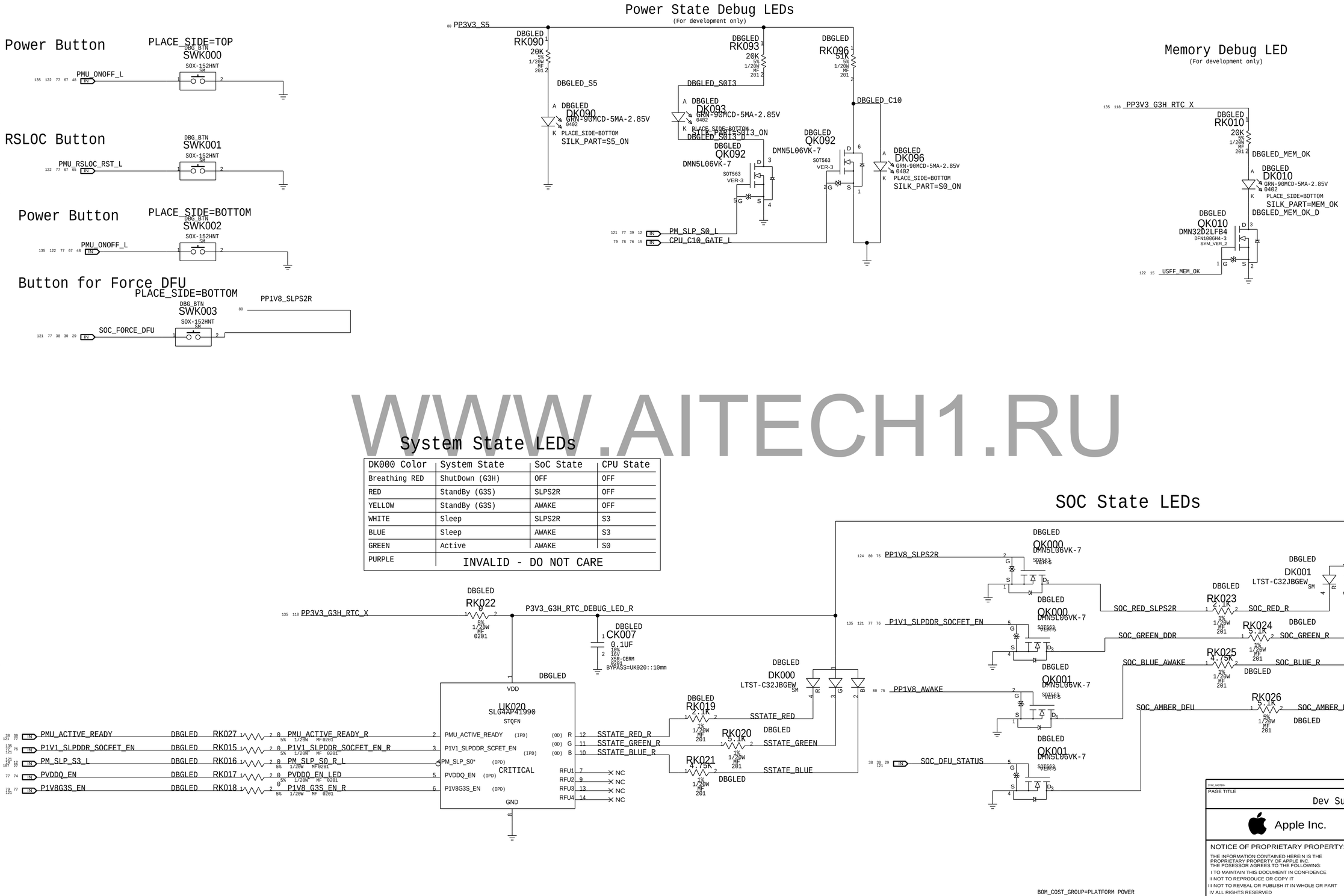

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